

INTEGRATION OF COMPLEX OPTICAL
FUNCTIONALITY IN A PRODUCTION
CMOS PROCESS

Thesis by

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My beautiful and loving wife has taken care of our energetic children for the last month while I've sequestered myself to write this document, and for this I am most grateful. She bankrolled our family when I left my paying job to become a graduate student, and she's tolerated the many years, relocations, and long hours it's taken to see this work accomplished. Without her love and support, none of this would have been possible.

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And, of course, it was Jon Osborn that brainwashed me with the silicon integration religion in the first place. Little did he know the chain of events that would sprout from decapping that ADXL50 back in '97.

ABSTRACT

Optical functionality has been developed within the confines of an existing CMOS process. As of this writing, 10Gigabit modulators, electrically tunable optical filters, waveguides, and grating coupler technology have been successfully implemented alongside the existing transistors in the Freescale Hip7SOI process. This technology will be used to manufacture high bandwidth optical interconnections directly on silicon chips, allowing a new type of network and computing infrastructure to be developed.

This work is covered in two distinct phases. First, the exploratory work done to gain experience with high index contrast silicon waveguides primarily served to uncover challenges related with simulation of these devices, and with the practical limitations of efficiently coupling the resulting waveguide devices with the outside world.

The second phase began as the grating coupler emerged to address the coupling challenge. It became feasible to conceive of a commercially viable technology based on silicon photonics. The coupler has been evolved to a high level, currently achieving coupling loss of less than 1dB. Once the light is on chip, filtering and modulation technology are implemented. The reverse-biased plasma dispersion modulator has a 3dB roll-off of 10GHz, and an insertion loss less than 5dB. Optical filters based on ring resonators, arrayed waveguide gratings, and interleavers have all been implemented, often with world record performance, and many of the devices have been made electronically tunable to compensate for manufacturing variations and environmental excursions.

Finally, circuitry has been designed and constructed on the same die with the optical functionality, fully demonstrating the ability to achieve monolithic integration of these devices.

TABLE OF CONTENTS

Integration of photonics components in CMOS	12
What this thesis work represents	13
Silicon always wins	14
Silicon as an optical material.....	15
Silicon Optical Constants.....	17
Complex Dielectric Constant.....	17
Polysilicon and Surface States	20
SOI CMOS processing.....	22
Integration with Fully depleted transistor technology	23
Partially depleted transistor technology.....	24
Summary of Technology Platform as of this writing.....	25
Overview of the Photonically Enabled CMOS Process	25
Switching Polarizer.....	27
Basic Device Design	27
Free carrier-effect calculations	29
Fabrication	29
Testing	31
Results and discussion	32
Ring resonator fabrication	33
Device Fabrication	36
Coupler Fabrication	38
Results and Discussion.....	41
Erbium doped light sources	41
Fabrication	42
Testing	43
Results and Discussion.....	46
Grating coupler simulations and theory	47
Grating Coupler Design Methodology	55
Grating Coupler Realization.....	62
Measurement technique	63
Wafer-scale Test.....	63
Ring resonators	65
Ring Resonators as Filters	65
Free Spectral Range.....	66
Single Pole Filter Design	66
Rings as Diagnostic Structures.....	70
Rings as Modulators.....	71
CMOS Modulator	73
Basic Free-Carrier Modulation Properties of Silicon.....	73
Diode Basics.....	76
The Waveguide	78

Modulator Measurement Results	81
Wafer Selection	84
Double Stack Wafer.....	84
Optimization Process	85
Dimensional Scaling.....	94
The Bandwidth Limitations.....	95

LIST OF FIGURES

<i>Number</i>	<i>Page</i>
Figure 1. a) The right hand side of this figure shows an arrayed waveguide grating, complete with optical phase shifters in each arm. On the left is a DAC for digital control of the individual phase modulators. b) The modulator driver (left side of figure b) is integrated with an optical modulator (right side). Only the launch end of the modulator is shown.	12
Figure 2. Transmission spectrum of optical fiber as it has evolved over time. Note that the region around 1.55 μ m is the low loss region, although for a 300m link, the loss is <1dB over the range 0.75-1.75 μ m.	16
Figure 3. Comparison of data from Herzinger (referred to as “This Work”) with previous measurement of silicon optical properties. Due to recent collection of this data (1998), and the advances in material purity, and measurement apparatus, this recent data is believed to be more accurate than past work.	18
Figure 4. Optical Properties of Silicon. This data is taken from a lightly p-doped silicon wafer using Variable Angle Spectroscopic Ellipseometry by Herzinger, et. al.	19
Figure 5. This figure shows the index of refraction over the useful fiber optics communications wavelengths from the bottom of the O-band through the top of the L-band.	20
Figure 6. Silicon (solid lines) versus polysilicon (dashed lines).	21
Figure 7. Measured Optical Properties of Polysilicon in the Telecommunications Range. Crystalline silicon data (dashed line) is given for comparison. The absorption of crystalline silicon could not be measured over this wavelength range.	22
Figure 8. Effective and group index for both polarizations of the first and second order modes of a silicon slab at $\lambda=1.55\mu$ m.	24
Figure 9. A cross-sectional diagram of key components of Luxtera’s technology implemented monolithically, and sharing the same processing steps.	26
Figure 10. A close-up SEM view of a portion of a silicon membrane patterned to form a polarizer. The cross-bar in the center of the picture was found to be necessary to prevent “stiction” of the beams together, and was repeated every 25 μ m. The total membrane was 100x100 μ m. The two orthogonal input polarizations are indicated by the arrows.	28
Figure 11. Fabrication steps involved in construction of a silicon membrane: a) silicon nitride etch mask is deposited on both sides of the wafer and patterned on the bottom. b) anisotropic etch of the silicon wafer using KOH c) etch of the buried oxide using HF d) removal of the nitride mask using boiling phosphoric acid e) application of PMMA mask, e-beam exposure and development and f) plasma stripping of mask.	30
Figure 12. Test setup used to evaluate the performance of the polarizer under the influence of modulation. The chopper provided the modulation signal to the grating, which was then correlated with the modulated 1550nm light via the lock-in amplifier. The white light source was used in conjunction with the camera to image the device for alignment of the IR beam.	31

Figure 13.	Data taken from switching polarizer. The power of the 633nm HeNe is shown on the right axis. Note that the transmitted power reaches a maximum when polarized orthogonal to the gratings, as expected. The left axis shows the OMA of the 1480nm laser, as detected by the lock-in amplifier.	32
Figure 14.	a) directional coupler optical motion transducer device concept. b) disk resonator version	34
Figure 15.	Drawing, approximately to scale, of the core of a single mode fiber (circle) compared to a 100x200nm waveguide (rectangle). This illustrates the problem associated with butt-coupling approaches often used to couple fiber with to larger waveguides.....	35
Figure 16.	Processing steps associated with fabrication of suspended silicon features: a) Starting SOI wafer b) deposition of oxide mask c) PMMA and Au deposited d) lithography and development of PMMA e) pattern transferred to oxide in RIE f) pattern transferred to silicon in ECR g) sacrificial removal of oxide, leaving suspended structures. Dimensions not representative of all structures in this work.	36
Figure 17.	Top and perspective views of a pair of silicon nano-mechanical beams fabricated in close proximity and suspended. Each beam measured 400x200nm, and was 10 μ m long.	37
Figure 18.	Top view of a die containing tapered waveguides etched in the top silicon film. A silicon pad is left in the center, so that ebeam defined devices can be formed.....	38
Figure 19.	Three separate attempts to align a 3 way splitter to the structure illustrated in Figure 11. In each case, note the alignment between the optically defined and e-beam lithography defined waveguides. In (a), the dark squares are charging of the oxide associated with SEM inspection of the misalignment.....	39
Figure 20.	Three devices fabricated with the intention of suspending the waveguides in order to optically measure the mechanical vibration. They are: a) a directional coupler, b) a Mach-Zehnder Interferometer, and c) a disk resonator.	40
Figure 21.	Cleaved endface of a SOI waveguide written with a stitching stage ebeam lithography system. Note the stage stitching error seen on the waveguide sidewalls. .	41
Figure 22.	Power density of the fundamental optical mode for a 300x300nm optical waveguide, with air cladding and glass cladding. The mode is extended into the glass as the index contrast is reduced, resulting in a confinement factor of 50% in the glass.	42
Figure 23.	a) Ring device fabricated for deposition of Erbium doped glass b) after deposition of glass. Device to be pumped from above.	42
Figure 24.	Photographs of a high quality disk resonator and a low quality ring resonator fabricated for Erbium deposition. Normally, sample a) would have been scrapped, but the defect structure allowed wafer normal test to occur.....	43
Figure 25.	Spectrum of Erbium implanted silicon dioxide deposited on top of a silicon waveguide, and pumped from above.	44
Figure 26.	Top: Resonance spectrum of a the ring without Erbium doped glass deposited. Bottom: After deposition. Note reduction in Q and reduction in extinction ratio of the ring after Erbium was deposited, indicating enhanced absorption.....	45
Figure 27.	Cross-sectional diagram of a grating coupler illustrating the scattering sites formed on top of a silicon film. Scattering sites can be deposited material, such as polysilicon, or features etched into the existing film. The buried oxide thickness is typically ~1 μ m thick.	47

Figure 28. k-space diagram for light incident on an air/glass interface from within the glass. The dashed line indicates the transverse wavenumber, which must be preserved in all allowed modes.	48
Figure 29. k-space representation of a transmission grating formed on a air/glass interface with the light incident from within the glass. Dashed lines represent the transverse wavenumbers of the supported diffractive orders.....	50
Figure 30. Cross-section of a slab waveguide and a 2D representation of the slab modes in k-space are represented by the points along the silicon circle. The dashed regions of the silicon circle represent regions where no TIR occurs, and waveguiding is not possible.....	51
Figure 31. k-space diagram illustrating grating diffraction and waveguide modes.....	52
Figure 32. k-space diagram illustrating the reverse coupling condition where only one mode is allowed in silicon.	53
Figure 33. Exponential radiation profile from a uniform grating.	55
Figure 34. Illustration of relationship between power decay in the waveguide (dashed) and ideal grating scattering strength.....	56
Figure 35. Radiation power scattered from a single “grating” deposited on a waveguide. Vectors indicate poynting flux through points along a box surrounding the grating. Note fraction of power scattered up.....	57
Figure 36. Scattering strength and phase shift as a function of grating width for both polarization modes of a slab waveguide. Note the nonlinear response of the functions. The vertical axis on the top figure shows both transmission and reflection coefficients for the two fundamental polarization modes of a slab waveguide. Scattered power is 1-T-R.....	57
Figure 37. A SEM photograph of a grating coupler formed from polysilicon gratings deposited on a hyperbolically flared silicon waveguide. The footprint of the grating represents a 10 μ m optical fiber mode. The output waveguide is 200x400nm.....	58
Figure 38. a) Destructive interference created by inappropriate choice of oxide thickness. b) Correct oxide thickness creates more efficient coupler. Any reflector will suffice, although DBR is shown.....	59
Figure 39. Simulation and experimental results from the first grating coupler design.....	63
Figure 40. A test loop consisting of two identical grating couplers, connected by a short waveguide. Spacing is 127 μ m.....	63
Figure 41. Photograph of wafer probe capability showing RF and low frequency electrical probes from the top and sides respectively. Optical fiber probe enters from the bottom of the picture. Fibers exit normally from the surface of the wafer and curve out of the picture on the left hand side. The wafer is the green surface below the probes.....	64
Figure 42. Wafer plot of peak grating coupler efficiency as an example of a benefit of wafer-scale testing.....	64
Figure 43. Ring resonator configured as an add/drop filter. The ring diameter is 5 μ m.....	65
Figure 44. Effective optical pathlength vs. cavity FSR, and the required cavity length for several interesting frequency spans.....	66
Figure 45. Filter shape of ring with Q=10,000. Adjacent channels plotted with dashed lines, demonstrating -20dB crosstalk with each adjacent channel.....	67
Figure 46. Data take from the drop and transmission ports of a ring filter.....	69

Figure 47. Transmission measurement of a $2\mu\text{m}$ radius ring, creating a 45nm (56THz) FSR. Inset shows measured ring and waveguide.	70
Figure 48. Spectrum of a corrugated ring showing critical coupling at the resonance order associated with the number of corrugations. Upper inset shows coupling region of ring structure. Lower inset shows close up view of deep resonance.....	71
Figure 49. Corrugated waveguide measurements (red dots) plotted with continuous curves extracted from ring measurements.	71
Figure 50. Time constant of a cavity as a function of Q for $1.55\mu\text{m}$ light.	72
Figure 51. Index modulation as a function of free carrier density from Soref's corrected formulas.	75
Figure 52. Absorption modulation as a function of free carrier density from Soref's corrected formulas.	75
Figure 53. Ratio of index modulation to loss by free carriers.....	76
Figure 54. Cross-sectional diagram of a generic modulator waveguide. Note, guiding mechanism not shown in order to focus on modulator itself.....	78
Figure 55. The movement of the total depletion width as a function of concentration and voltage. Shown for $-0.5, 1, 2, 3$, and 4V	79
Figure 56. Cross-sectional view of a silicon modulator. The optical mode is shown along with the overlap with the implants. This does not reflect doping in the ridge portion, although the ridge is typically doped as well.	81
Figure 57. Test setup for the high-speed modulator.	82
Figure 58. Spectra of a high speed modulator using an unbalanced MZI taken at different voltages.....	82
Figure 59. Modulator phase shift as a function of DC voltage for a 5mm device.....	83
Figure 60. Frequency response measurement and 10Gb eye diagram for a reverse biased modulator.	84
Figure 61. Cross-section of a double stack wafer. A thin oxide breaks the top silicon electrically, but maintains single mode operation optically.	85
Figure 62. The 5 wafer options considered for production implementation.....	87
Figure 63. Comparison of frequency response and 10G modulator eye diagrams on different wafers.....	91
Figure 64. Grating coupler insertion loss over the C-band. Top line indicates best simulation result. Other lines are measurements showing evolution over time.....	92
Figure 65. Waveguide loss for the nominal waveguide width of $0.5\mu\text{m}$, compared to waveguides $1\mu\text{m}$ and $3\mu\text{m}$ wide. Note the decreasing loss with additional width. The 500nm width is guaranteed to provide single mode operation. The average loss is 1.8dB for this configuration. Inset: A waveguide "scroll" used in varying lengths to extract loss.	93
Figure 66. Scaling for dimension of each 10G transceiver assuming numerous 10G transceivers are used to attain a significantly higher unidirectional bit rate. Based on a 1sqcm die.	94
Figure 67. Fundamental limitations of silicon photonics technology from a materials and media perspective. The bandwidth between the blue lines represents the addressable bandwidth, $\sim 45\text{THz}$. This can be extended by straining the Ge to redshift the absorption edge by approximately 10THz	95

LIST OF TABLES

Table 1. Summary of the known techniques for coupling into high-index waveguides, arranged in order of popularity.....	46
Table 2. Simulated impact of substrate reflectivity on peak efficiency of an example grating coupler. Wafer factor refers to the number of reflective layers in the substrate. The negative number indicates a perfectly out of phase condition.	60
Table 3. Composite ranking of waveguide performance by wafer type.....	88
Table 4. Ranking of grating coupler efficiency for the wafer types.	89
Table 5. Wafer types ranked by key modulator performance parameters.....	89
Table 6. Final ranking of the different wafer types.....	90

INTRODUCTION TO SILICON PHOTONICS

Integration of photonics components in CMOS

As of this writing, this line of research has been underway for 7 years, and the technology has been developed with a high degree of success. Today CMOS circuit designers and optical engineers work together to create monolithically integrated functions, such as 10Gigabit optical modulators integrated with the driving amplifiers, and electronically tunable Arrayed Waveguide Gratings (AWGs) as shown in Figure 1.

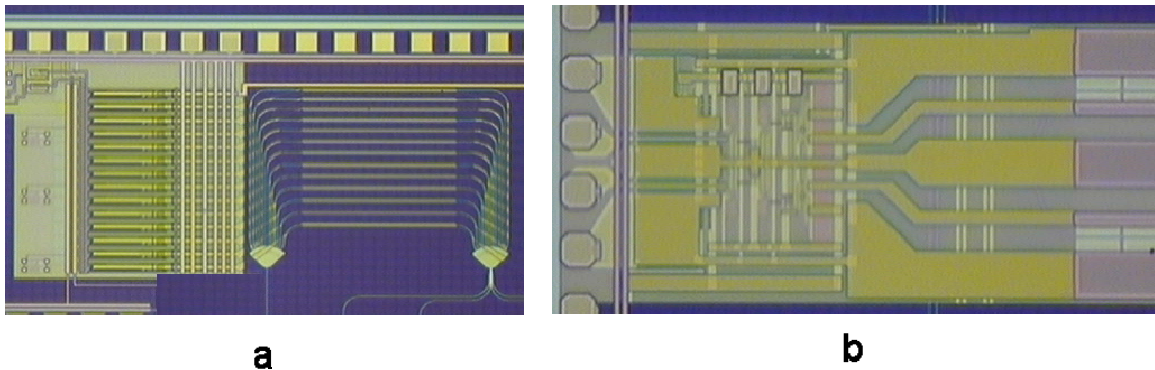


Figure 1. a) The right hand side of figure a shows an arrayed waveguide grating, complete with optical phase shifters in each arm. On the left is a DAC for digital control of the individual phase modulators. b) The modulator driver (left side of figure b) is integrated with an optical modulator (right side). Only the launch end of the modulator is shown.

Complex functions integrated into a single die were only a conceptual goal when this work was started, but today product development is underway where digital functionality, RF circuitry, and optical capabilities are monolithically integrated. This thesis will cover some of the key developments as the technology was nurtured from an embryonic concept to a promising young technology with high commercial potential. Today's technology is aimed at high

bandwidth connections in high performance computing and networking systems. As the technology continues to mature, there is substantial promise for integration of optical transceivers directly onto communications limited die, such as network processors, microprocessors, memory, and communications hubs. In addition, there are a number of non-traditional applications where this technology has promise, such as optical sensing and coherent optical communications.

Intra-chip communications between blocks in a single die are perhaps the ultimate example of CMOS integration, requiring cost and power performance directly competitive with copper traces, and a level of design integration that allows optical functionality to be implemented in a transparent manner. Regardless of the trajectory that this technology takes, the explosion in interest and investment in silicon photonics over the last few years ensures that this field will be interesting to watch in the coming years.

What this thesis work represents

This work is separated into two distinct phases, divided by the founding of a company, Luxtera, aimed at commercializing the technology. Work prior to Luxtera was performed exclusively in the Nanofabrication Group facilities at Caltech, where conception, design, fabrication, and test all occurred serially, and almost exclusively by the hands of this author. This work is characterized by cleanroom processing details, basic simulations, and optical bench test setups commonly seen in this type of thesis. The goal was to get a few “hero” devices fabricated and tested, and to learn a great deal about the silicon photonics platform as a result. Early devices were the switching polarizer, and Erbium glass clad ring resonators. This work served more to uncover the problems and deficiencies of the technology than to truly push the state of the art. But this exposure to the true deficiencies of the Silicon photonics platform led to the concepts embodied in the founding of Luxtera.

The work at Luxtera took the early concept of a technology platform and rapidly pushed it towards a commercially realizable, CMOS integrated fabrication process. In order for this to occur, an enormous number of architectural and device decisions had to be made. Thus, the work during this phase is characterized by identification of the key technical issues, and

collection of information required to make those decisions. This involved designing thousands of devices that were all included in a single maskset, which was subsequently made at Luxtera's fabrication partner, Motorola (which later became Freescale Semiconductor). These devices would then be tested and analyzed, and additional improvements were identified. This process was repeated a number of times, with increasing complexity, until successful integration was achieved.

As this work proceeded, the level of effort scaled from a single graduate student in the lab at Caltech, to a 35 person company closely partnered with a giant CMOS production facility. Thus, work at Caltech, and in the early stages of Luxtera will be primarily reflected as hands-on design, fabrication, testing and analysis of specific devices.

In the later stages, the body of work is too extensive to be accurately captured here, and the large number of people required to undertake such an endeavor necessarily meant that this author's role evolved from sole contributor, to team leader. As such, the final portions of this thesis will focus on several key technical concepts and decisions closely directed by this author, and on the data and analysis required to make them.

At all stages of this development, this author played a key role in conception and innovation of specific optical devices, certain design aspects, and process integration techniques. While there are no published papers supporting this work, there are a large number of issued and pending patent applications covering this technology. As of this writing, the author has been awarded 4 US Patents [62-65], and has approximately 50 applications pending.

Silicon always wins

The late 1990s saw the reemergence of compound semiconductor electronics, driven originally by defense work, but commercially driven by companies such as Vitesse Semiconductor. Despite a narrow lead maintained by the compound semiconductors in key performance parameters, silicon technology continued to keep pace, particularly with SiGe becoming mainstream. By 2000, it was clear that silicon technology was not going to be threatened by GaAs or InP based technologies.

At the same time a new field of research, called Micro-Electro Mechanical Systems (MEMS) was a burgeoning field, drawing substantial investment from both private and government funding organizations. At the height of the excitement around MEMS technology, Analog Devices announced their ADXL50, a fully integrated MEMS accelerometer, aimed at the airbag sensor market. This product integrated a MEMS sensor device with all of the required circuitry and passive components to monolithically implement an accelerometer, complete with transducer, signal processing and control analog electronics, and digital readout.

Another data point around the same time was the emergence of the CMOS camera into a mainstream product capable of competing with the historically favored CCD cameras. While both of these technologies were embodied in silicon, the CMOS camera took the additional step of being based on CMOS transistor technology, instead of the boutique process required for CCD construction. The success of this technology over time is a testament to the power of integration into CMOS.

The combination of these events seemed to predict that silicon, particularly as embodied in the CMOS process, was going to continue to evolve in capability and maintain dominance in the traditional electronics markets, based on merits from both technical performance and commercial viability. This trend motivated the research aimed at integration of complex optical functionality into a CMOS process. First, basic research was needed to understand what type of silicon devices would be required, and what level of performance would be able to be achieved.

Silicon as an optical material

Silicon was first identified as medium for integrated optics by Dr. Richard Soref at the Air Force Rome Labs. Through a series of papers [1-4], Dr. Soref outlined the basic properties of silicon, particularly those that can be used for modulation effects. While silicon has a substantial Raman effect and a noticeable Kerr effect, the property that most easily sets silicon apart from the rest is the plasma dispersion effect, created by free carriers in the material. While this effect exists for any semiconductor, silicon is unique in that it has been extensively characterized, and is supported by an enormous and sophisticated manufacturing base.

Silicon's high index contrast poses unique challenges and possesses certain key benefits. The major benefit is that small waveguides can be constructed, well below $1\mu\text{m}$ in all dimensions. As a result, the bend radius and real-estate consumption of these waveguides makes them compatible with the layout requirements of CMOS processing. Their small cross-section is also an important factor in the speed and efficiency of free-carrier based modulation, which is clearly limited by geometric concerns related to carrier movement.

The transparency window of silicon also aligns well with the free space wavelengths used in communications systems today, $1.3\mu\text{m}$ and $1.5\mu\text{m}$.

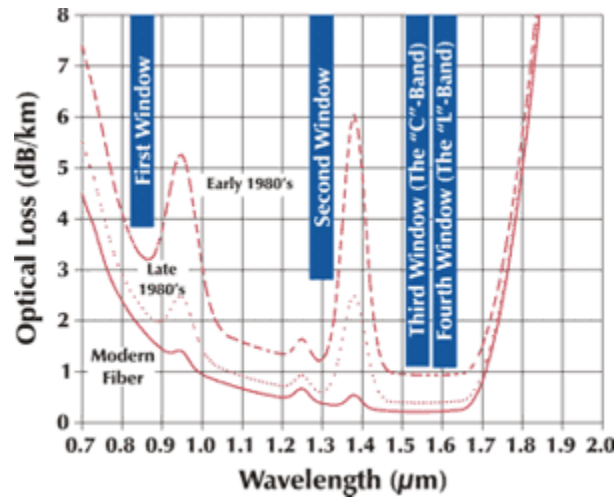


Figure 2. Transmission spectrum of optical fiber as it has evolved over time. Note that the region around $1.55\mu\text{m}$ is the low loss region, although for a 300m link, the loss is $<1\text{dB}$ over the range $0.75\text{--}1.75\mu\text{m}$.

The silicon bandgap at 1.1eV begins to strongly absorb light at $\sim 1.2\mu\text{m}$, while light above $1.6\mu\text{m}$ is absorbed by lattice scattering [5]. Experimental evidence taken at Luxtera and elsewhere confirms that $1.5\mu\text{m}$ light experiences the least amount of absorption in Silicon. This corresponds with the optical C-band, which is traditionally used for telecommunications in single-mode fiber due to the low attenuation of $< 0.25\text{dB/km}$. The alignment of the low attenuation wavelengths in fiber and silicon is a coincidence begging for exploitation.

Silicon Optical Constants

The optical properties of silicon, or any material, are intrinsically linked to its electronic states. In fact, almost every interaction of light with matter can be explained by examining how the electrons behave in the presence of the light's electric and magnetic fields. Thus, the same properties that make silicon interesting as an electronic material are responsible for making it an interesting optical material. As a semiconductor, silicon's electronic properties are highly dependent on crystallinity, temperature, and the presence of impurities, and likewise for the optical properties. While this is not the appropriate place to derive the full semiconductor theory of silicon, we will consider those aspects that are particularly relevant for optics.

Complex Dielectric Constant

Perhaps no other fundamental optical property is more important than the complex dielectric constant, ϵ , which despite the name, is not constant at all. $\epsilon(\omega)$ is a function of frequency and is directly related to the polarizability, $\chi(\omega)$, by

$$\epsilon(\omega) = 1 + 4\pi\chi(\omega)$$

In general, the dielectric constant is written in terms of a real and imaginary part,

$$\epsilon = \epsilon_r + i\epsilon_i$$

Similarly, the complex refractive index, \tilde{n} , is given as

$$\tilde{n} = n + ik$$

where the extinction coefficient, k , is related to the absorption coefficient, α , by $k = \alpha\lambda/4\pi$, where λ is the wavelength of light in free space. These complex terms are related by

$$\tilde{n} = \sqrt{\epsilon}$$

Thus, two practically important values, the real index of refraction, n , and α can be directly attained from the dielectric constant. These parameters are related as:

$$n = \sqrt{\frac{\epsilon_r + \sqrt{\epsilon_r^2 + \epsilon_i^2}}{2}}$$

$$\alpha = \frac{4\pi}{\lambda} \sqrt{\frac{-\epsilon_r + \sqrt{\epsilon_r^2 + \epsilon_i^2}}{2}}$$

Surprisingly, only during the last few years has accurate data been reported for the dielectric constant of crystalline silicon. See Herzinger, et al. [6]. This recent data has taken advantage of improvements in measurement techniques and equipment, and is more accurate than previous work, which often conflicted and was only reported over a limited wavelength range.

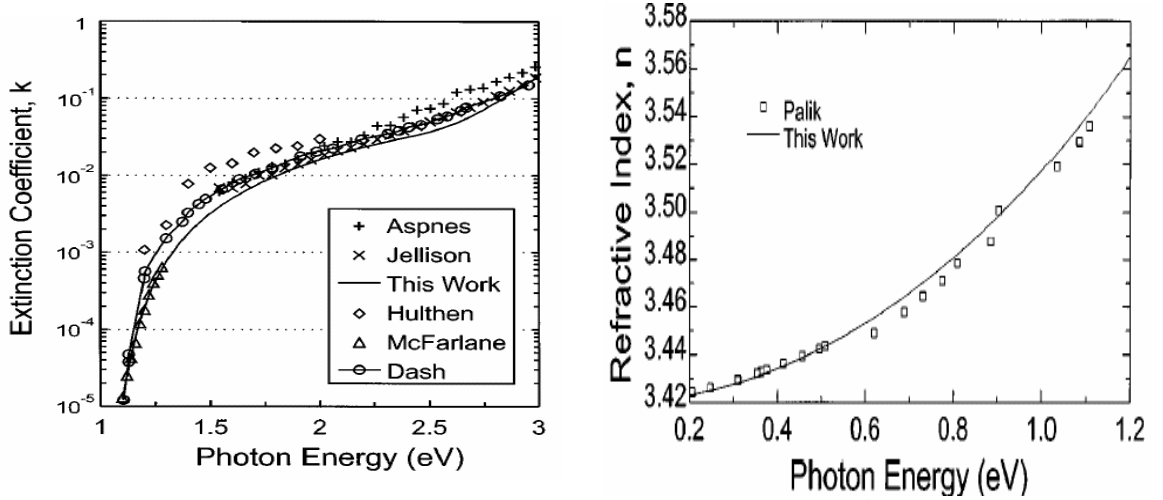


Figure 3. Comparison of data from Herzinger (referred to as “This Work”) with previous measurement of silicon optical properties. Due to recent collection of this data (1998), and the advances in material purity and measurement apparatus, this recent data is believed to be more accurate than past work.

Complete data over the useful optical range is given in Figure 4. This data is converted from the complex dielectric constant values given by Herzinger, and the extinction coefficient has been converted to the more useful absorption coefficient, as described in the equations above.

In addition, data for the refractive index is plotted over the useful fiber optics communications wavelengths in Figure 5. Note that the absorption coefficient has not been measured for these

wavelengths, and is assumed to be negligible over the distances commonly used in integrated optics. Also, it's apparent that a material dispersion of about 1% occurs over this range.

There's also some concern about the change of index due to surface states and stress induced by these surfaces. While this has not proven to be an issue on thin films of silicon, it's likely a concern with the sub-micron, single-mode waveguides etched from silicon. However, there is not a satisfactory way to measure this effect, since errors in film thickness and waveguide geometry cannot be measured with enough precision at these dimensions to separate out the effect of surface states on the bulk index.

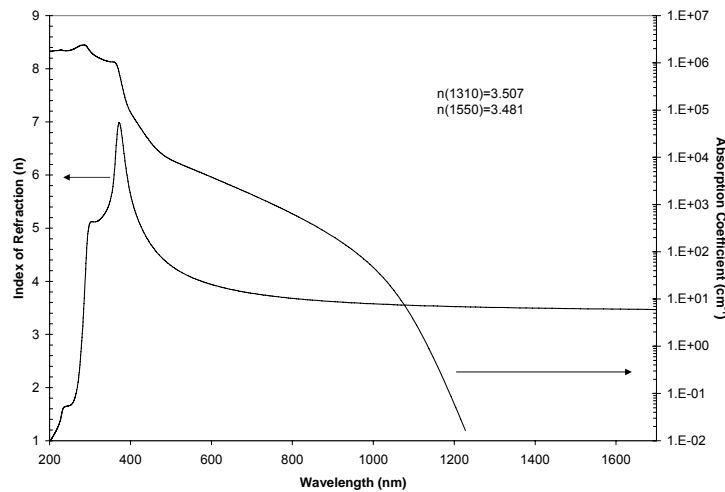


Figure 4. Optical Properties of Silicon. This data is taken from a lightly p-doped silicon wafer using Variable Angle Spectroscopic Ellipseometry by Herzinger, et. al.

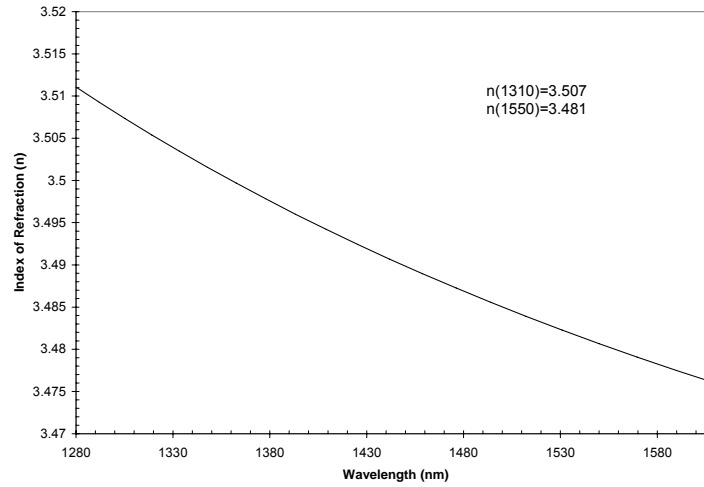


Figure 5. This figure shows the index of refraction over the useful fiber optics communications wavelengths from the bottom of the O-band through the top of the L-band.

Interestingly, there have been reports [7-9] of the optical properties of very thin film Silicon on Sapphire (SOS) and Silicon on Insulator (SOI) films that indicate a substantial shift in optical properties, although the age of the SOS result, in particular, casts the accuracy of the measurement into question.

Polysilicon and Surface States

Silicon is also commonly found in polycrystalline form, typically used for gates in CMOS processes. Due to the strain, surface states, and random crystalline orientation of the silicon grains in polycrystalline material, the optical properties are substantially impacted.

A polycrystalline sample was prepared by first growing a 100nm thermal oxide on a lightly p-doped silicon wafer. Next, 150nm of polysilicon was deposited by LPCVD using the standard procedures for constructing polysilicon gate films. Measurements of the polysilicon material were taken using a Woollam VASE, and the results are reported here.

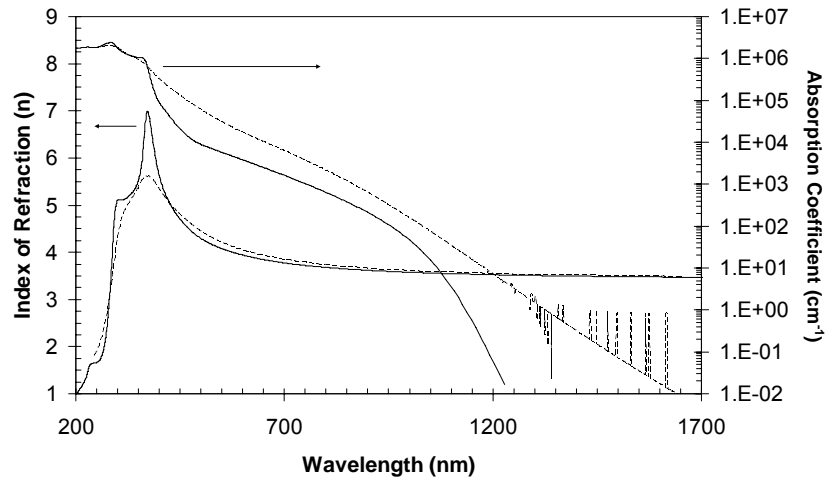


Figure 6. Silicon (solid lines) versus polysilicon (dashed lines).

As shown in Figure 6, polysilicon has a substantially higher absorption coefficient at all wavelengths outside of the UV. In particular, at the telecommunication wavelengths, the absorption coefficient is no longer negligible. Also note that the sharp features present above the bandgap in the refractive index of the crystalline silicon are smoothed out in the polycrystalline material.

Within the communications wavelengths shown in Figure 7, polysilicon has an index shift of ~ 0.02 higher than crystalline silicon, although the dispersion of the material has the same basic shape.

The spikes apparent in the absorption coefficient data are probably noise due to the sensitivity of measurement in the low loss regime, however, many of the spikes consist of several data points, and for this reason, they were not removed from the data. It's possible that some sort of optically resonant effect with the polycrystalline structure was producing local absorption anomalies. There is also a ripple present on the refractive index data with $\sim 7\text{nm}$ periodicity, which corresponds to a cavity of ~ 500 microns in silicon. This could be attributed to the thickness of the silicon wafer, which is neglected during the ellipsometry calculations.

It's important to realize that this data was taken from light passing through the plane of the film. Due to the columnar nature of the polysilicon film growth, this light saw fewer grain

boundaries than light traveling within the plane of the film would see. For this reason, it's likely that, for waveguided light, both the index difference and absorption coefficient are underestimated with this measurement.

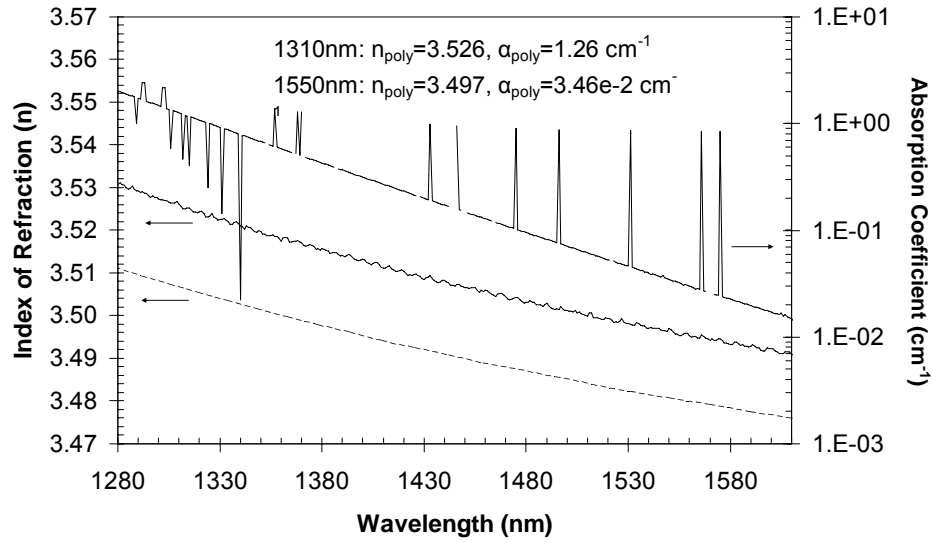


Figure 7. Measured Optical Properties of Polysilicon in the telecommunications range. Crystalline silicon data (dashed line) is given for comparison. The absorption of crystalline silicon could not be measured over this wavelength range.

In fact, previous measurements [8,9] of amorphous and polycrystalline films have yielded very high absorption coefficients which were greatly reduced upon annealing to increase the grain size.

SOI CMOS processing

The two aspects of silicon manufacturing that make it useful for optical structures are the recent emergence of Silicon-On-Insulator (SOI) wafers, and the progression of DUV lithography below the quarter wavelength of light in these waveguides. Single mode waveguides of the type developed in this work tend to have an effective index of refraction, n_e , between 2.5 and 2.8. Taking the least favorable end of that range, the quarter wavelength is

$$\frac{\lambda_0}{4n_e} = 0.138\mu m$$

thus it's no accident that the technology became viable with the advent of 0.13um CMOS processing. Once the technology node was identified for integration into CMOS, it was important to carefully consider the transistor technology of that node.

SOI transistors come in two basic flavors, depending on how far the gate depletion region extends into the body of the transistor. Transistors where the depletion region does not fully deplete the body of charge are called "partially depleted," and their counterparts are called "fully depleted transistors." The selection of which transistor to use is of critical importance to the optical properties of the technology because of the strong dependence on the thickness of the film employed. All SOI transistors have a distinct advantage when it comes to parasitic effects, such as parasitic capacitances associated with the body of the transistors, although fully depleted devices are slightly superior in this regard. Since the substrate has been replaced with an oxide, parasitic capacitance associated with the junctions in the substrate is greatly reduced.

Integration with Fully depleted transistor technology

Fully depleted transistors are generally considered superior, but at the voltage levels in 0.13um CMOS, the films required are approximately 50nm thick. For light of 1550nm, this means that waveguides constructed in this technology would be well below the single mode cutoff thickness of ~250nm.

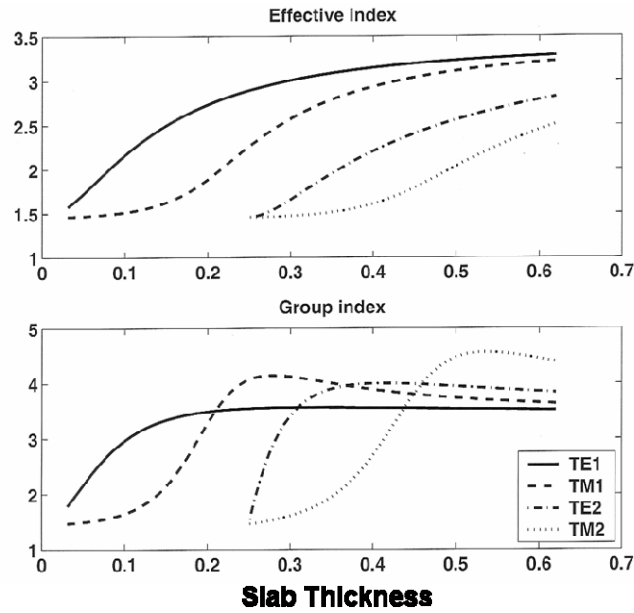


Figure 8. Effective and group index for both polarizations of the first and second order modes of a silicon slab at $\lambda=1.55\mu\text{m}$. The slab thickness is given in microns.

As a result, the optical mode would be extended well outside of the silicon film, requiring a very thick cladding on top and bottom of the film, and detrimentally impacting the bend radius of the waveguide. Additionally, since the modulation scheme envisioned required injection of carriers in the silicon, it was desired to have more of the light confined in the silicon. Thus, integration with FD SOI requires additional complexity in the wafers, such as the double stack solution discussed in Chapter 3.

Partially depleted transistor technology

PD SOI transistors are typically constructed in SOI films between 70 and 250nm thick. These transistors will have charge underneath the channel when the transistor is operating, creating non-ideal transistor behavior, such as the “kink” effect. For digital circuitry, this effect is tolerable, and perhaps even advantageous in certain situations, but for analog and RF circuitry, the kink poses a design problem. A common approach used to address this concern is to integrate a body tie to the layout of each individual transistor. This makes the layout slightly larger, and poses limitations on the allowed gate width of high frequency transistors. Since

many optical components require high-performance analog and RF circuitry, consideration of this effect must occur during the selection of the CMOS process and will impact the wafer chosen for implementation.

Summary of Technology Platform as of this writing

While this author cannot take sole responsibility for the current state of the technology, it is important to consider the present level of performance of the components described herein, if only for a testament of their potential for commercial success. Much of the original work done during the early stages of this activity could be questioned with regard to the relevance, or the ability, of the technology to scale to the point that the use becomes practical. It is hoped that a brief summary describing the current capabilities will put such concerns at rest.

Overview of the Photonically Enabled CMOS Process

A key feature of the technology is that the components are monolithically fabricated, in close proximity, within a single die, in such a manner that allows each device to function well. This is not a trivial task, as the processing steps for constructing a grating coupler are completely shared with those processing steps for a modulator, which are shared for the processing steps for the transistors. The true breakthrough that Luxtera has made is the demonstrated ability to realize such a wide variety of devices simultaneously. Figure 9 shows a cross-sectional diagram of the current Luxtera process. Note that the same films, etches, and lithographic patterns used to form the transistor can be shared among the other devices. A common shallow trench isolation etch has been introduced to simultaneously define the grating coupler etch depth, the passive waveguide confinement, and the modulator confinement, as well as the modulator contact resistance.

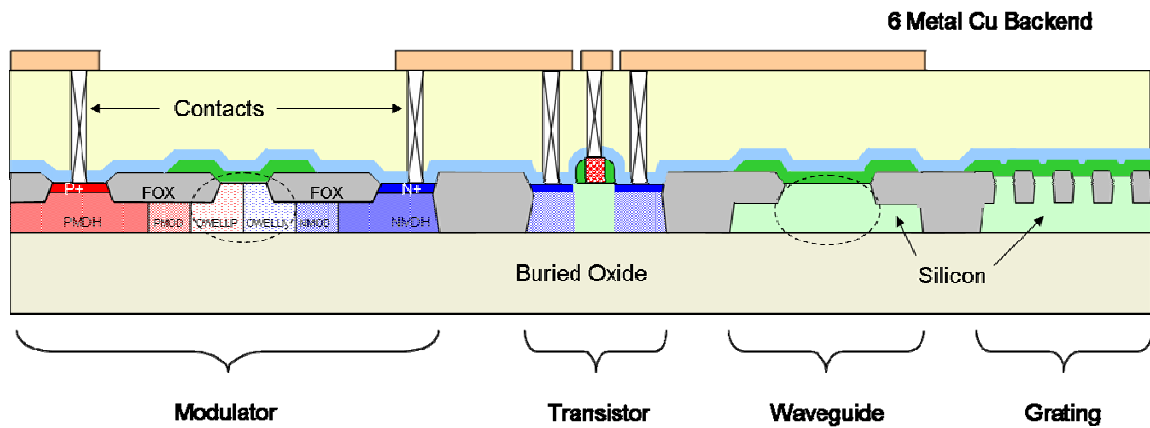


Figure 9. A cross-sectional diagram of key components of Luxtera's technology implemented monolithically, and sharing the same processing steps

A complex tradeoff space regarding wafer dimensions, transistor performance, grating coupler efficiency, and modulator bandwidth has been undertaken, and an optimization point has been found that allows each and every one of these components to function with the required performance levels in order to commercialize the technology. As of the time of this writing, the process is capable of monolithically integrating transistor circuitry, 10Gb modulators, grating couplers, directional couplers, y-junctions, electronically tuned arrayed waveguide gratings, electrically tuned interleavers, ring modulators, tunable ring filters, and a host of similar waveguide based devices.

EXPLORING SILICON PHOTONICS

The work covered in this section spans June 1998 through late 2001, and was performed at Caltech, primarily in the facilities of the Nanofabrication Group. Three key devices constructed during this period will be discussed, a switching polarizer, passive ring resonators, and Erbium clad active ring resonators.

Switching Polarizer

A diagram of a switching polarizer is shown in Figure 10. Collimated light is passed through the plane of the device, which is configured as a transmissive, absorption-based polarizer. Such polarizers are constructed of sub-wavelength conductors, aligned parallel. When light with the electric field polarized parallel to the conductors is incident, electron movement is excited in the conductor, which experiences resistive loss, making the film opaque. When light of the orthogonal polarization, aligned transverse to the conductors is applied, no excitation of the carriers is created, allowing the light to pass through without attenuation.

Basic Device Design

It would be advantageous to have the ability to modify the degree to which light of a particular polarization passed through such a polarizer, so a semiconductor version of this device was conceived. A thin film of silicon would be etched to create a number of closely spaced, though isolated, silicon lines. Modification of the conductivity of these lines would allow absorption of a single polarization of light to be modified as it was passed through the device. Due to the complexities of electronic-based modification of the conductivity, it was decided to generate free carriers by photopumping of the silicon polarizer. Thus, electron-hole pairs would be created which would contribute to the conductivity of the lines. In order to separate the effects of the bulk substrate, the device would require MEMS-style suspension on a thin membrane.

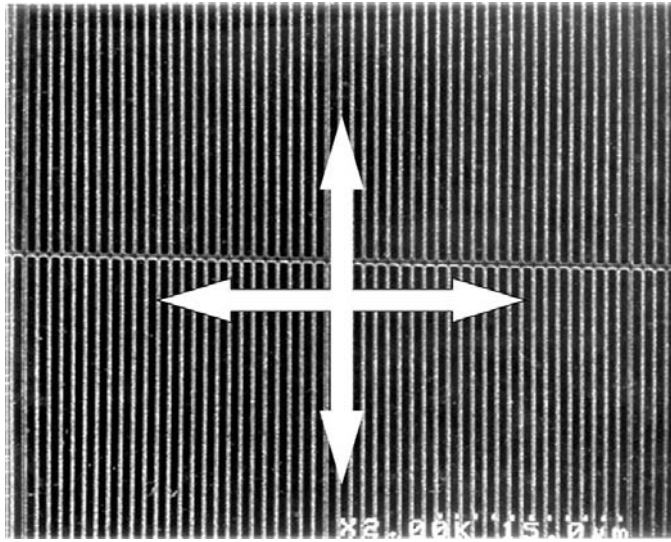


Figure 10. A close-up SEM view of a portion of a silicon membrane patterned to form a polarizer. The cross-bar in the center of the picture was found to be necessary to prevent “stiction” of the beams together, and was repeated every $25\mu\text{m}$. The total membrane was $100\times 100\mu\text{m}$. The two orthogonal input polarizations are indicated by the arrows.

For convenience, light of 633nm was chosen as the pump wavelength, and light from an Erbium pump laser of $1.48\mu\text{m}$ was chosen as the signal wavelength. To be compatible with materials on hand, a silicon film thickness of 200nm was used.

In order to avoid diffractive effects on the signal wavelength, the pitch of the grating must be chosen to be under the free-space wavelength of the light. Thus, a $1\mu\text{m}$ pitch was chosen. Additionally, it was desired that the cross-section of the grating members be less than the wavelength of light in that material. Using this criteria, a 300nm cross-section was chosen.

In order to test this device in free-space, a $100\mu\text{m}$ wide aperture was desired. Due to the mechanical instability of a suspended grating feature 300nm wide and $100\mu\text{m}$ long, a support beam was placed every $25\mu\text{m}$. From prior experience, this was known to be long enough to support the grating, while occupying a negligible amount of surface area of the grating to interfere with the orthogonal polarization.

Free carrier-effect calculations

Silicon under illumination by 633nm light has an absorption coefficient of 2900cm^{-1} , as can be seen in Figure 6. In a 220nm thick film, this equates to 6.2% absorption of the incident light. Taking into account reflections at the front and back surfaces of the film results in absorption of just under 3% of the incident light. Furthermore, only 30% of the film surface is remaining after patterning, leaving an absorption factor of 1%. Thus, with a measured incident laser power of 4mW, only 40 μ W was absorbed in the silicon.

A 633nm photon contains ($E=h\nu$) 3.14×10^{-19} J, meaning that 1.3×10^{14} photons/sec were being absorbed. This power was dissipated in a volume of silicon 0.01mm^2 , by 220nm thick, and only 30% populated, resulting in an e-h pair generation density of 8.5×10^{23} e-h pairs/ cm^3/sec . The carrier lifetime eventually sets the steady state carrier concentration under illumination, and in these small structures surface recombination was expected to play the dominant role in the carrier lifetime, resulting in a small expected lifetime, postulated to be $\sim 1\text{ns}$. Under these conditions, the carrier concentration under illumination would be 10^{14}cm^{-3} . This should create a small modification of the conductivity of the silicon, though not a dramatic effect as will be seen in the later section concerning free carrier modulation.

Fabrication

An SOI wafer from Silicon Genesis Corporation was acquired. The top silicon film of the wafer was 220nm, and it was separated from the substrate by 400nm of buried oxide. The substrate was 525 microns thick. CVD deposition of 60nm of Si_3N_4 was performed on both sides of the wafer by a commercial vendor, which was subsequently segmented into die, each about 0.5cm^2 via the scribe and break technique. Then, photolithography was performed on the back of die, which was exposed and developed to reveal a square feature centered on the back. The Si_3N_4 in the exposed area was etched via ECR. After this was performed, the photoresist was removed in stripper solution, and the die were cleaned to prepare for the KOH anisotropic etch.

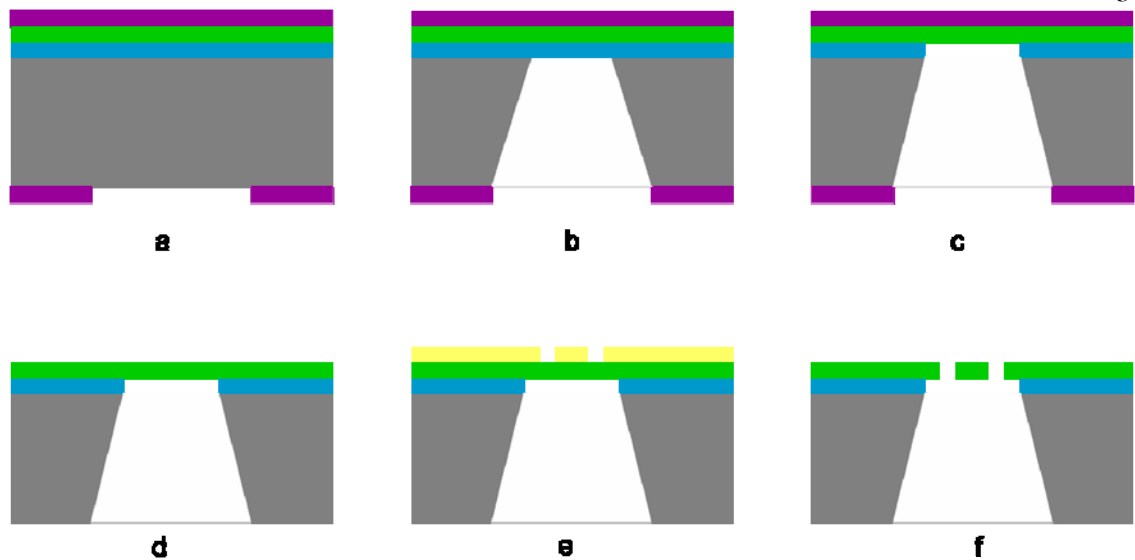


Figure 11. Fabrication steps involved in construction of a silicon membrane: a) silicon nitride etch mask is deposited on both sides of the wafer and patterned on the bottom. b) anisotropic etch of the silicon wafer using KOH c) etch of the buried oxide using HF d) removal of the nitride mask using boiling phosphoric acid e) application of PMMA mask, e-beam exposure and development and f) plasma stripping of mask

The KOH etch was performed in a solution made from 30% anhydrous KOH pellets and 70% water, by weight. The solution was brought to a boil, and was calibrated to etch $1\mu\text{m}$ per minute. Due to the $525\mu\text{m}$ thickness of the wafer, a 9 hour etch process was required. After removal from the KOH solution, the die were placed in boiling phosphoric acid for 5 minutes to remove the silicon nitride.

The resulting die contained a membrane, formed from silicon and silicon dioxide. A 10 sec. submersion in HF, followed by ethanol, removed the remaining silicon dioxide leaving a simple silicon membrane.

At this point, the membranes were observed to be substantially deflected down from the surface, though they proved to be surprisingly strong. The die could be vacuum chucked during the deposition of the PMMA without rupturing.

PMMA was spun on this film, and e-beam lithography was performed. The PMMA was developed, and the die was etched using a XeF_2 process. After the XeF_2 was completed, the die was placed in an O_2 plasma for 30 min. to strip the PMMA. The resulting die contained a suspended structure, as shown in Figure 11.

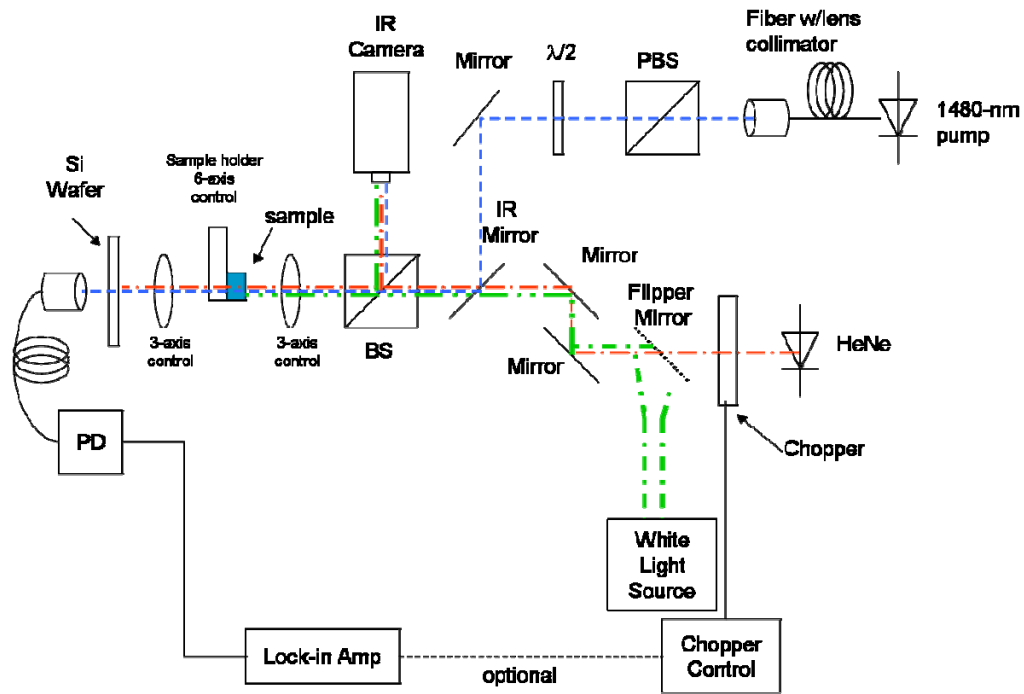


Figure 12. Test setup used to evaluate the performance of the polarizer under the influence of modulation. The chopper provided the modulation signal to the grating, which was then correlated with the modulated 1550nm light via the lock-in amplifier. The white light source was used in conjunction with the camera to image the device for alignment of the IR beam.

Testing

A test setup was constructed as shown in Figure 12. The die was placed on an aluminum plate, machined to fit in a lens mount, and with the membrane centered over a small hole drilled through the plate. Using the half-wave plate, the polarization of the 1480nm signal light incident on the sample was rotated. A chopper was placed in the path of the pump light, and the signal from the chopper was synched with the lock-in amplifier. The room was blackened, and the signal strength was measured as a function of polarization. Both the DC signal, and the lock-in signal were recorded and are shown in Figure 13. By independently blocking the

signal and pump beams, it was confirmed that the measured output was a result of their interaction in the membrane structure.

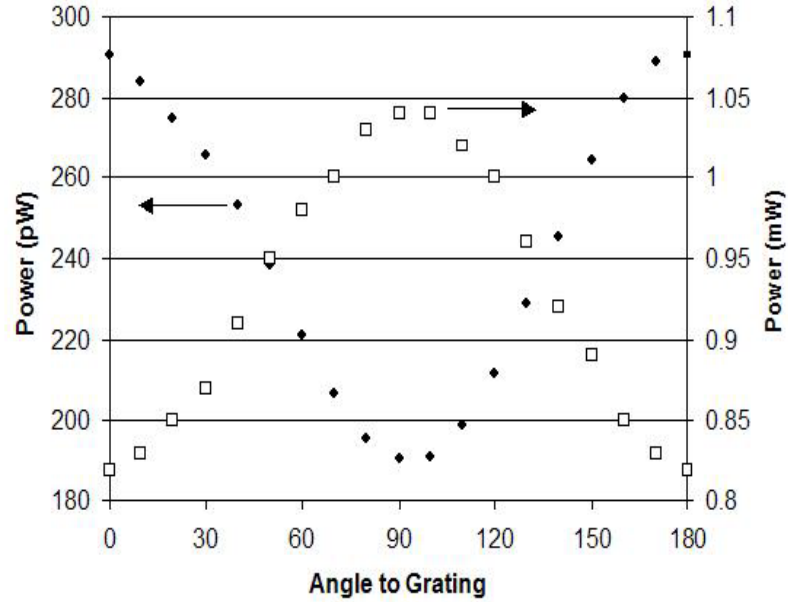


Figure 13. Data taken from switching polarizer. The power of the 633nm HeNe is shown on the right axis. Note that the transmitted power reaches a maximum when polarized orthogonal to the gratings, as expected. The left axis shows the OMA of the 1480nm laser, as detected by the lock-in amplifier.

As shown in the DC output, the structure acts as a polarizer, resulting in peak transmission when the light is polarized orthogonal to the grating structure. At this point, the magnitude of the modulation is less, as expected. When the light is aligned with the grating, the transmission drops to a minimum, although the effect of the modulation is greatest at this point. This effect was verified through several repeated measurements of the sample over the course of a week. Due to the faint nature of the output signal, the integration time of the lock-in amplifier, was set up to 100s, resulting in a time-consuming measurement.

Results and discussion

This experiment successfully demonstrated polarization dependent modulation of light. The fact that the modulation was polarization dependent confirms that the modulation was not simple absorption, but was related to the fine structure of the grating. However, the

performance of the device was not at levels that were exciting from a practical perspective. Granted, there is substantial room left for improvement of this device. First, the film could be substantially thicker. This would allow greater absorption of the pump light, and thus, a higher carrier generation rate. Additionally, the thicker film would increase the carrier lifetime, creating a higher carrier density under illumination. Also, surface treatments, such thermal oxidation or forming gas annealing could be used to increase carrier lifetime.

A preferred way to produce the same effect is to use electrical modulation instead of optical pumping. It is hypothesized that an increased effect would be seen in this situation, were carrier concentrations can be modified at substantially higher levels than those used achieved in this work. For example, MOS capacitor structure, formed in the shape of a grating could be used to accumulate charge underneath the gate, rapidly forming a conductive structure suitable for absorption of a single polarization. Additionally, it would be possible to form an interdigitated p-n diode, which would have the conductivity of the film modified by forward or reverse-biasing. At levels of adequate reverse bias, the film would contain no conductive structure what-so-ever, which would be an improvement over the MOS capacitor approach, where the gate structures would serve as a polarizer independent of the applied voltage.

Though this device served as proof-of-principle, due to the poor performance and lack of an exciting real-world application, it was decided to not conduct further experiments on this device, and to move on to waveguide structures, where the interaction length of the light and the material could be made substantially longer.

Ring resonator fabrication

The first motivation for the ring or disk resonator was to employ high-Q optical cavities as a sensor for quantum effects. Such experiments had been proposed by Braginsky [10]. According to his calculations, sufficiently high Q resonators could be used to transducer vibration by exploiting evanescent coupling between the optical resonator and an adjacent structure, such as a waveguide or another resonator. The basic concept for the experiment is shown in Figure 14. Light would be coupled into a waveguide, which would be suspended in close proximity to a disk resonator, or configured as a directional coupler. Due to the rapid

decay of the evanescent field of a high-index contrast waveguide, the evanescent coupling is an extremely sensitive function of position. Thus, it was desired to maximize the transverse wavenumber to enhance the sensitivity of the transducer. Additionally, the high Q of the ring allowed for resonant behavior, which would serve to enhance the sensitivity of the measurement.

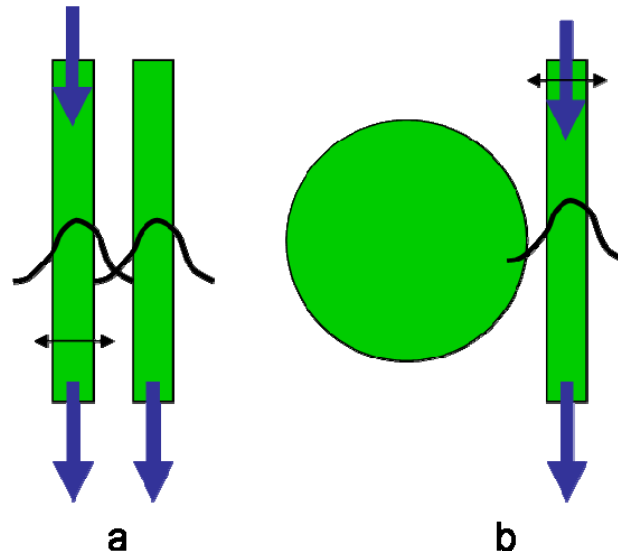


Figure 14. a) directional coupler optical motion transducer device concept. b) disk resonator version

The beam would be suspended using a selective etch removal process, which would create a pillar underneath a disk or ring resonator, and would allow the waveguide to move with respect to the ring. The entire apparatus would be placed in a cryogenic refrigerator in order to quench native thermal effects. The incoming light would be modulated with a swept frequency. As the optical field built up in the resonator, the ponderomotive force between the resonator and the waveguide would be used to excite mechanically resonant vibrations in the waveguide. It was desired to explore the level of accuracy with which the mechanical motion could be transduced, and to eventually verify Braginsky's prediction of observation of quantum phenomena.

However, a large number of technical challenges remained to be overcome before such an experiment could be realized. First, these devices containing submicron features must be fabricated, and secondly, light must be coupled into these devices with enough efficiency to allow the measurement to be made. Neither of these tasks is trivial. Figure 15 illustrates the mechanical relationship, to scale, between the core of single mode fiber and the waveguides envisioned for this experiment, which must be minimal in cross-section. As one can see, the coupling efficiency between the two waveguides is necessarily extremely small. Based on cross-sectional area ratios, a typical estimation technique, -27dB of light would be lost, both upon entering and leaving the waveguide. Such losses would pose a dramatic problem inside a cryogenic environment, as the lost power would become heat as the light was absorbed on the chamber walls.

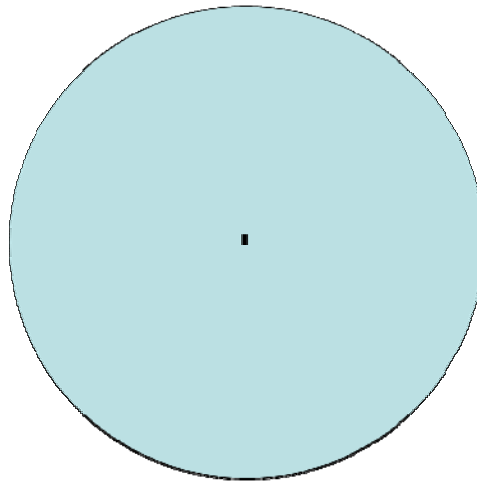


Figure 15. Drawing, approximately to scale, of the core of a single mode fiber (circle) compared to a 200x400nm waveguide (rectangle). This illustrates the problem associated with butt-coupling approaches often used to couple fiber with to larger waveguides.

Thus, the problem was divided into a two step development activity. First, the process to fabricate the devices would be developed, and second, a process allowing more efficient waveguide coupling would be developed.

Device Fabrication

A key problem with device fabrication was that no etch process existed capable of using PMMA as a mask to etch silicon. Thus, due to the high selectivity between silicon dioxide and silicon in an ECR Chlorine plasma process, and the availability of this tool, a hard mask based fabrication process was targeted, as shown in Figure 16. In this process, a SOI wafer is used as the starting point, and an oxide is either grown or deposited on top of the wafer. At this point, PMMA is applied, followed by a flash of Au on top of the PMMA. The Au is essential to shield the electron beam from charging of the oxide layer experienced during writing. After patterning and development of the PMMA, a RIE etch is performed to pattern the oxide. At this point the PMMA is removed and the part is transferred to the ECR etching chamber where the silicon etch is performed. After this step, a wet oxide etch is used to suspend the part, followed by a critical-point drying process to avoid deformation of the part experienced during evaporation of the solvents.

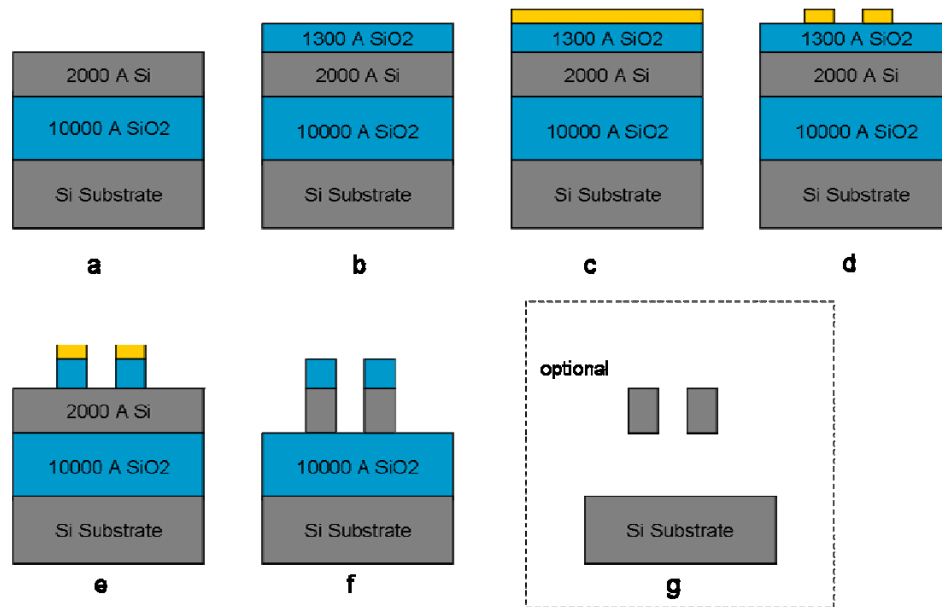
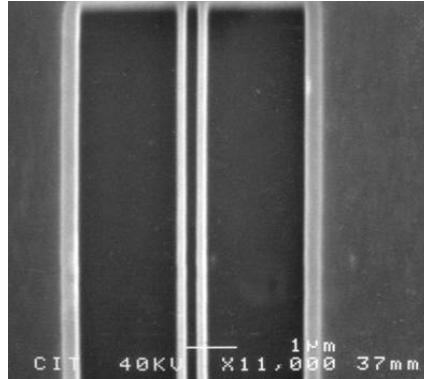
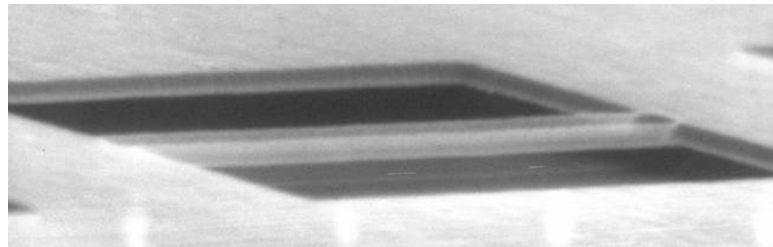


Figure 16. Processing steps associated with fabrication of suspended silicon features: a) Starting SOI wafer b) deposition of oxide mask c) PMMA and Au deposited d) lithography and development of PMMA e) pattern transferred to oxide in RIE f) pattern transferred to silicon in ECR g) sacrificial removal of oxide, leaving suspended structures. Dimensions not representative of all structures in this work.

The first attempts at device fabrication focused entirely on the suspended portion of a directional coupler device. This device was chosen for the complexity of processing steps required in construction, as it was expected to be a worst case example, requiring submicron resolution over a long distance, and successful suspension of two structures within close proximity to each other.



top view



perspective view

Figure 17. Top and perspective views of a pair of silicon nano-mechanical beams fabricated in close proximity and suspended. Each beam measured 400x200nm, and was 10μm long.

Using the processing steps outlined above, this device was successfully created as shown in Figure 17. The separation between the waveguides was 200nm, and each waveguide was 200nm wide and 400nm thick. The aspect ratio of the waveguides was chosen to be 2:1, so that the mechanical resonance would be preferred in the mode that resonates in the direction of the other waveguide instead of towards the substrate. The SEM photographs show clean

etching and removal of the oxide. Additionally, the two waveguides are cleanly separated from one another, and not bound together as often happens during removal of the oxide from the substrate.

Once the fabrication process for the transducer devices had been established, attention was turned to development of a technique for coupling light into these small devices.

Coupler Fabrication

The design of the coupler was complicated by the fact that ebeam lithography could only be performed in a $100 \times 100 \mu\text{m}$ square with adequate resolution to resolve the desired devices. Thus, an approach was devised where traditional photolithography would first be employed to fabricate large, multimode waveguides that would extend to the perimeter of a die, and which would connect to an unpatterned region of silicon in the center of the die. This pattern is shown in Figure 18. The top silicon film of the SOI wafer would be etched away in all regions except the waveguides, alignment marks, and the center pad. In order to allow for alignment for the ebeam lithography step, the central pad was chosen to be $40 \mu\text{m}$ square, and the corners of the SEM field of view would be used for alignment.

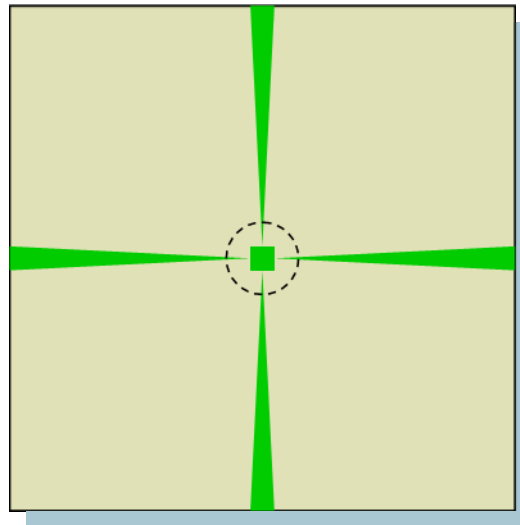


Figure 18. Top view of a die containing tapered waveguides etched in the top silicon film. A silicon pad is left in the center, so that ebeam defined devices can be formed.

In order to test this approach, a simple 3-way splitter was first designed. This splitter would allow verification of a 4 port device, such as a directional coupler or MZI constructed from 2 directional couplers.

Using the alignment marks left from the first processing step, the ebeam pattern was written on the central pad, which was etched to form the completed devices. Several resulting devices are shown in Figure 19. Despite numerous attempts at this type of device construction, alignment between the original waveguides and the final waveguides could not be achieved with sufficient accuracy.

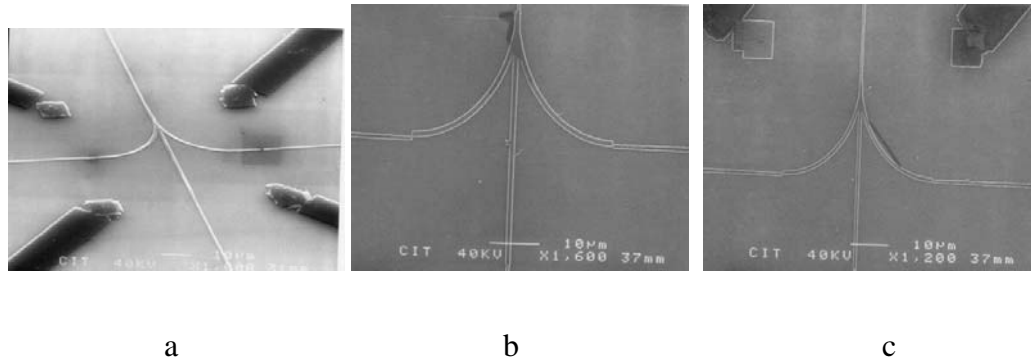


Figure 19. Three separate attempts to align a 3 way splitter to the structure illustrated in Figure 18. In each case, note the alignment between the optically defined and e-beam lithography defined waveguides. In (a), the dark squares are charging of the oxide associated with SEM inspection of the misalignment.

Thus, this technique was abandoned for a second approach that did not require a two-step process. Instead, the structures would be fabricated to contain a 90° bend in the waveguides, and would be fabricated in a small area in the center of a die. The die would subsequently be cleaved along two axes, exposing the input and output waveguides to the edge of the die. At this point, the die would be placed in a mechanical alignment stage, and polished fibers, or high numerical aperture optics, could be brought to each edge of the die for coupling.

A number of devices were constructed to test the approach, as shown in Figure 20, parts a-c. In each case, the area of the device intended for suspension is shown by the dashed lines. Despite the success in device fabrication, the cleaving and testing of these devices proved to be

a substantial challenge. A vast majority of fabricated devices were destroyed at the cleaving step, due both to the inaccuracy of cleaving an SOI substrate, and the tendency of the top film to flake during cleaving, resulting in a ragged waveguide edge. Finally, it was discovered that mechanical alignment stages were available for waveguides that were constructed in-line, with light entering one side of a chip and exiting opposite. However, alignment of the chip and two sets of coupling optics within an area of 50 μ m square would require design and development of custom stages, and would not be compatible with the cryogenic environment required for final measurement of the device.

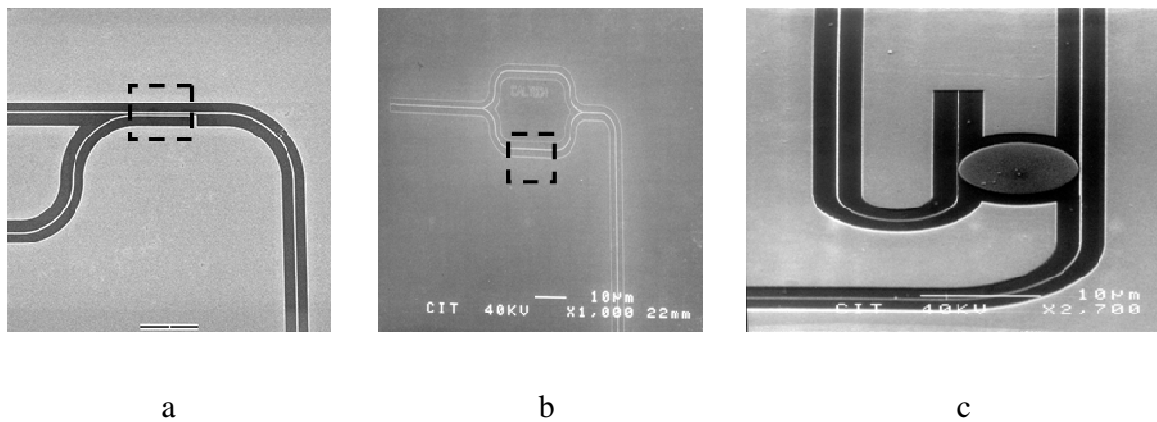


Figure 20. Three devices fabricated with the intention of suspending the waveguides in order to optically measure the mechanical vibration. They are: a) a directional coupler, b) a Mach-Zehnder Interferometer, and c) a disk resonator.

Another approach was to outsource the ebeam lithography process to a more capable facility, which would employ a moving stage capable of stitching fields together. This technique allows extension of the waveguides over a region large enough to be successfully cleaved, in principle, allowing waveguides to be fabricated many millimeters long. This approach was attempted using the ebeam lithography system at JPL. A cross-section of a resulting device is shown in Figure 21. This figure shows the cleaved facet at the end of one such waveguide. Note that while the stage is capable of high alignment precision, stitching errors are not negligible. While this waveguide is 1 μ m wide at the edge of the die, resulting in a multimode waveguide for ease of alignment, the waveguides required for the transducer devices are much smaller at the center of the die. This stitching error turned out to be too high for single mode operation.

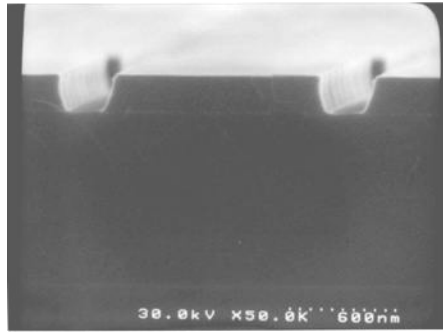


Figure 21. Cleaved endface of a SOI waveguide written with a stitching stage ebeam lithography system. Note the stage stitching error seen on the waveguide sidewalls.

Results and Discussion

This concludes the attempts to use SOI waveguide devices for mechanical transducers. In summary, this effort successfully yielded device fabrication processes, and a number of high-quality nanofabricated devices, although measurement was not practical. This highlighted a fundamental issue with the development and construction of high-index contrast photonics – it was essential to develop a technique to get light on and off the chip before the technology could be practical, even for academic purposes. Rather than embark on an effort to build a hero device by many repeated attempts, it was decided to solve the problem by generating light on the die.

Erbium doped light sources

During modeling of the high index structures required in the above work, the cladding of the waveguides was necessarily air or vacuum. However, as shown in Figure 22, if a glass cladding was applied to the waveguides, the index contrast of the waveguide surface would be reduced, shrinking the transverse wavenumber, and allowing a substantial amount of the optical power to be guiding in the cladding. In fact, calculations using FDTD indicated that for a 300nmx300nm glass-clad waveguide, 50% of the light was in the cladding.

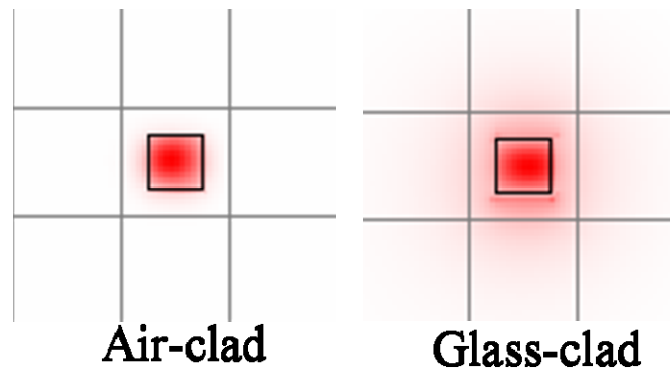


Figure 22. Power density of the fundamental optical mode for a 300x300nm optical waveguide, with air cladding and glass cladding. The mode is extended into the glass as the index contrast is reduced, resulting in a confinement factor of 50% in the glass.

This realization lead to the concept of an erbium-doped glass cladding, which could be pumped surface normal in addition to resonant pumping. In either case, amplification occurs through overlap with the evanescent field and the excited Erbium. This concept is shown in Figure 23.

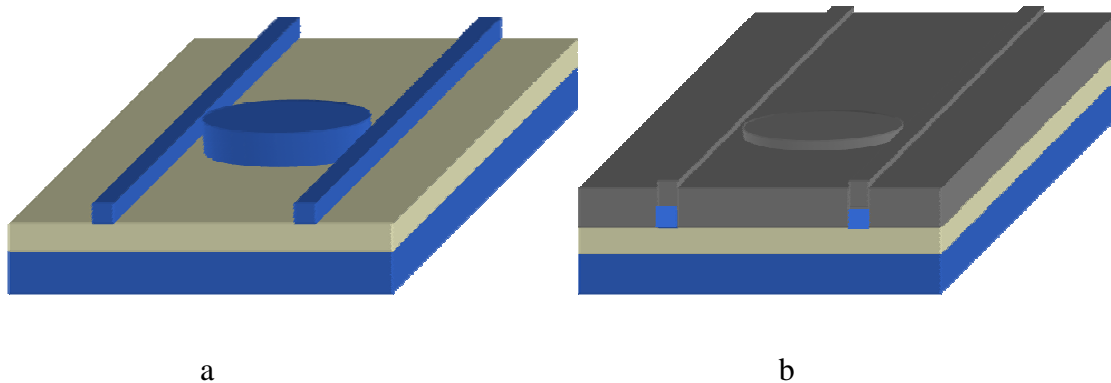


Figure 23. a) Ring device fabricated for deposition of Erbium doped glass b) after deposition of glass. Device to be pumped from above.

Fabrication

The major drawback of this design is that a new fabrication process had to be developed. In the prior process, an oxide hardmask had been relied upon for etching of the optical

structures. This hardmask can not be removed without undercutting the oxide underneath the waveguides. Since the field concentration is highest close to the waveguide, this region required deposition of Erbium material, so a technique must be devised that did not require the use of a hardmask. The approach chosen was to construct a XeF_2 etching system, which was known to have a low etching rate in PMMA as compared to silicon.

A CAIBE system was modified with a XeF_2 chamber, which consisted of a stainless steel chamber clad in heating tape. XeF_2 tablets were introduced to the chamber, though under heat and vacuum, they were converted into gas and introduced to the CAIBE chamber via a mass flow controller, essentially taking the place of the Chlorine typically found in such systems. After the etching step was performed, the PMMA could be removed in a combination of solvents and oxygen plasma stripping.

At this point, an oxide cladding was deposited by spin-on-glass, which contained Erbium in varying concentrations. Additional samples were constructed by reactive sputter deposition of silicon dioxide, followed by implantation of Erbium. Pictures of two fabricated device are shown in Figure 24.

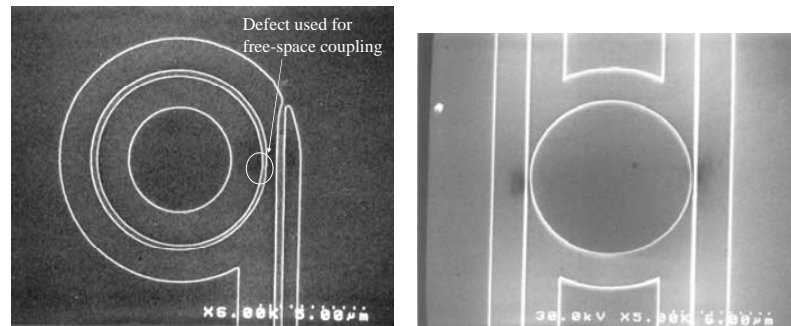


Figure 24. Photographs of a high quality disk resonator and a low quality ring resonator fabricated for Erbium deposition. Normally, sample a) would have been scrapped, but the defect structure allowed wafer normal test to occur.

Testing

In order for the devices to work properly, it was essential that a resonant pump be employed, however, this work was being done at the height of the telecommunications bubble, and as

such, there was more than a 1 year lead time for erbium pump lasers. Thus, other approaches were employed for more immediate testing of the constructed devices.

For an initial test of these devices, they were pumped from above using a variety of light sources. A fiber was placed at the output of the single waveguide, and was sent to either a photodetector, or an optical spectrum analyzer, as desired. No emission was observed from the spin-on-glass samples. The erbium implanted samples did show a weak erbium luminescence, as shown in Figure 25.

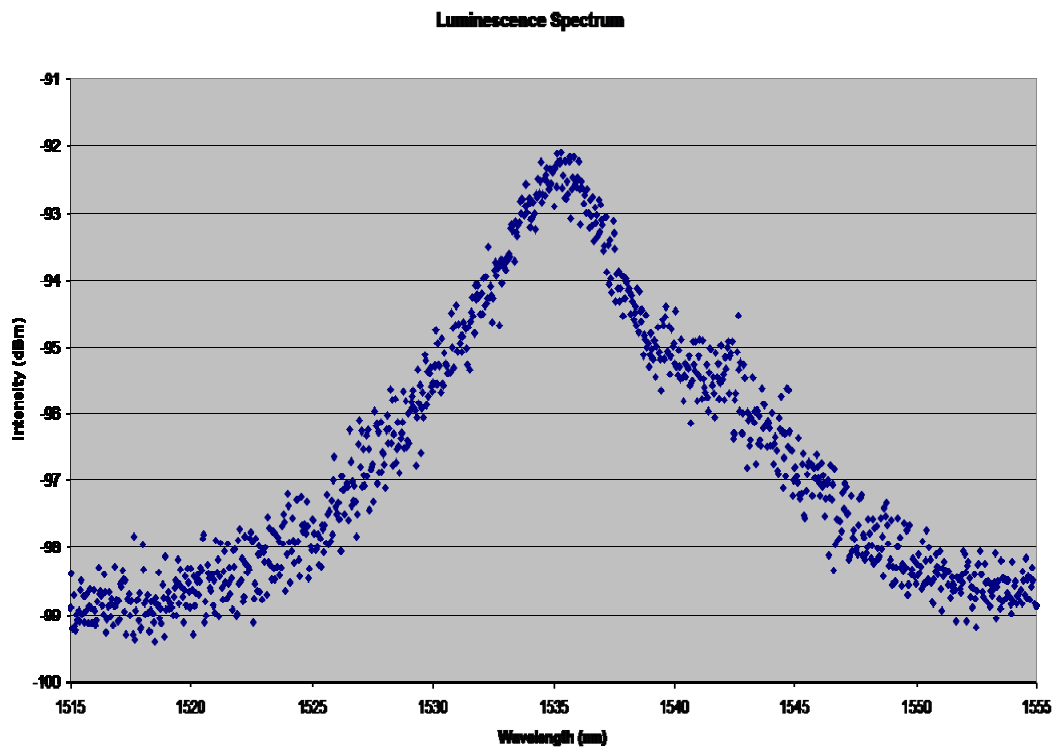


Figure 25. Spectrum of Erbium implanted silicon dioxide deposited on top of a silicon waveguide, and pumped from above.

One of the main suspects for the limited device performance was high waveguide loss, resulting in a small Q for the cavity. In order to explore this hypothesis, a testing technique commonly employed to evaluate photonic crystal cavities was explored. This approach was not expected to work for waveguide devices, which do not have the numerous scattered

modes found in photonic crystals. However, the accidental fabrication of a device with a clear defect in the ring raised the question about coupling into the resonator through use of a scattering site. This approach was successful, and did not require alignment to the output waveguide. Figure 26 shows the resonant spectrum observed from this measurement, both prior to and after erbium doped glass deposition. Note that the defect scattering site present in the ring adversely impacts the Q of the ring, and as such, the measured Q is substantially below the required value of 20,000.

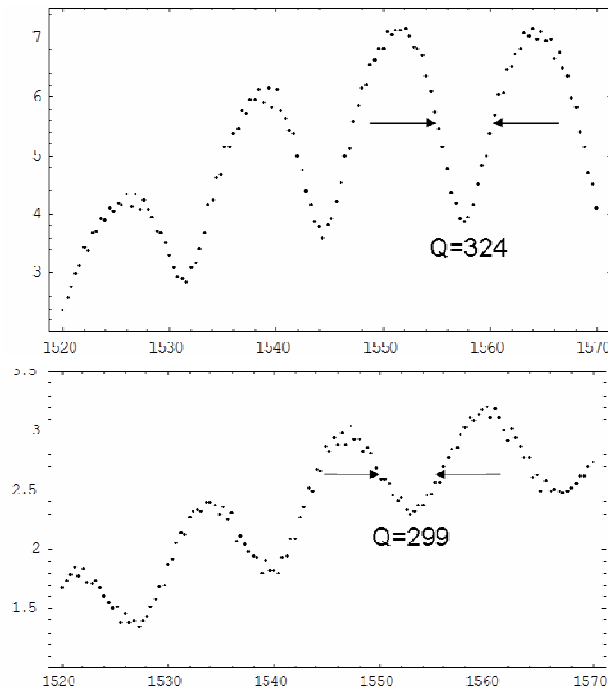


Figure 26. Top: Resonance spectrum of a the ring without Erbium doped glass deposited. Bottom: After deposition. Note reduction in Q and reduction in extinction ratio of the ring after Erbium was deposited, indicating enhanced absorption.

It's clear from the pictures of the fabricated devices that the sidewall quality is not sufficient for low-loss operation. This is a fundamental drawback of ebeam lithography techniques, which tend to result in a rough surface due to the small diameter of the electron beam.

Results and Discussion

While it had been proven that some light could be generated on chip, it was not an efficient process, and the lack of available pump lasers dramatically limited the feasibility of such work. None the less, coupling from the top of the chip, and specifically, by using scattering sites in a waveguide, had proven to be an effective and rapid technique for evaluation of a device. The next step was to place the scattering site on a waveguide, which would then be used to couple to a defect free resonant cavity. However, this technique appeared to have very little coupling efficiency, and a better approach was desired.

At this point, a survey of all known coupling techniques was undertaken to develop a better approach for coupling into the small waveguides required desired for high-index contrast silicon waveguides.

	General Popularity	Geometry	Efficiency	Bandwidth	Ease of Test	Ease of design	Ease of die fabrication	Potential for CMOS Compatibility
High NA Optics	1	Edge	Poor	Good	Horrible	Good	Good	Good
Lensed Fiber	2	Edge	Marginal	Good	Hard	Good	Good	Good
Flared taper	3	Edge	Good	Good	Marginal	Marginal	Hard	Bad
Narrowed taper	4	Edge	Marginal	Good	Hard	Marginal	Good	Marginal
Prism Coupler	5	Top	Good	Good	Hard	Good	Good	Bad
Grating Coupler	6	Top	Poor	Poor	Good	Horrible	Hard	Great

Table 1. Summary of the known techniques for coupling into high-index waveguides, arranged in order of popularity.

Table 1 is a compilation of the known techniques for coupling light into high-index waveguides. Each technique listed in the leftmost column, in order of perceived popularity, was evaluated with respect to its coupling geometry, coupling efficiency, bandwidth, testability, ease of design, ease of fabrication, and the potential for CMOS compatibility. Note that the first 4 techniques are all edge coupling approaches, and had been previously attempted without

great success. Of the remaining two, the prism coupler showed little promise for eventual integration into CMOS. The final option, the grating coupler, was known to be inefficient, narrowband, and extremely difficult to design and fabricate. However, the potential for surface normal testing, which eliminates the need for edge preparation, was a substantially appealing, leading to the decision to explore this device further.

Grating coupler simulations and theory

The grating coupler was an extension of the concept used in the prior section for measurement of the ring resonator through a scattering site. However, careful construction of an array of scattering sites, similar to a phased-array antenna, could effectively provide “antenna gain,” allowing a higher coupling efficiency to be achieved [19]. This is the basic principle behind grating coupler design, and while difficult, it has been demonstrated that this technique has the potential to be over 90% efficient over several THz of optical bandwidth.

A grating coupler is quite simply an array of scattering sites placed in sequence down a waveguide, as shown in Figure 27. For an optical mode traveling in the waveguide, each scattering site has a scattering efficiency, radiation profile, and a phase delay for transmitted light. Knowledge of these parameters allows calculation of the emitted optical field, which can then be analyzed for mode matching with the external optics, such as an optical fiber.

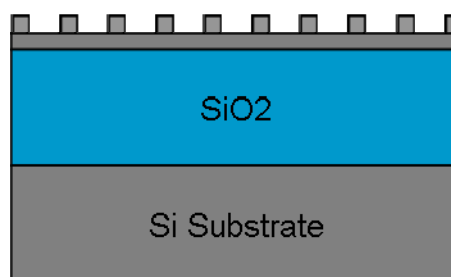


Figure 27. Cross-sectional diagram of a grating coupler illustrating the scattering sites formed on top of a silicon film. Scattering sites can be deposited material, such as polysilicon, or features etched into the existing film.

A simple conceptual model based on k-space phase matching requirements was developed to set the basic requirements for a grating coupler design, and will be described in detail in the next section.

A useful diagram for understanding grating coupler operation is the k-space diagram, as shown in Figure 28 for a simple air/glass interface. For most circumstances, a 2D generalization of the grating coupler can be considered, so the majority of the k-space diagrams will only show two dimensions.

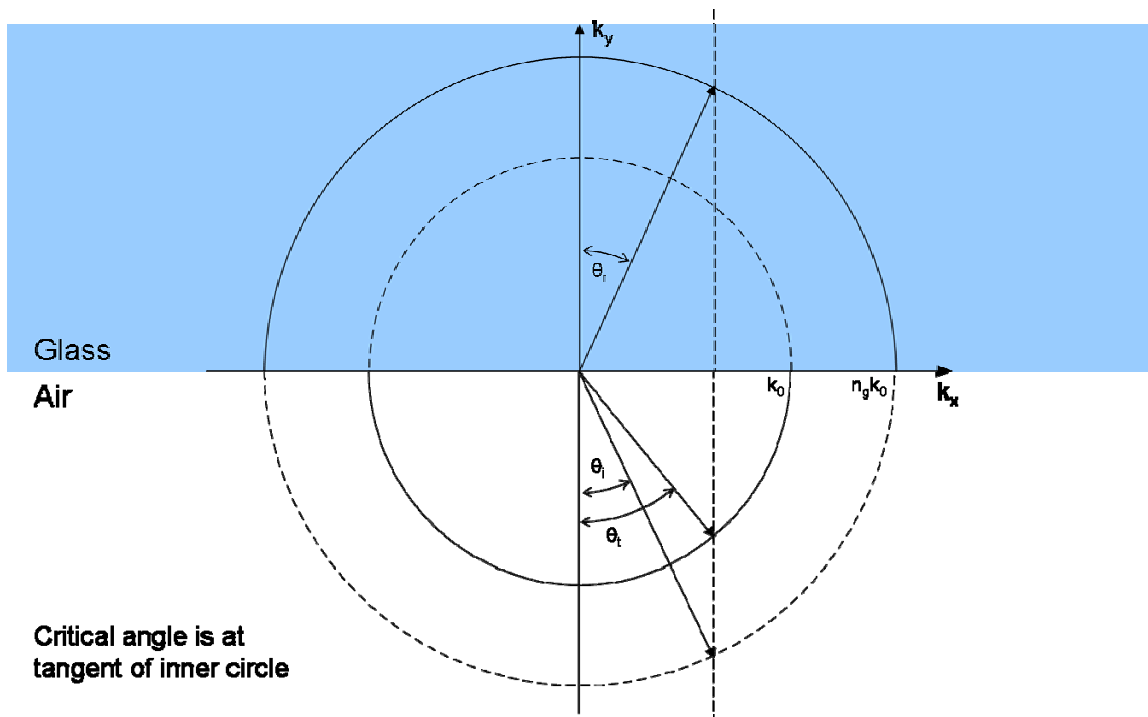


Figure 28. k-space diagram for light incident on an air/glass interface from within the glass. The dashed line indicates the transverse wavenumber, which must be preserved in all allowed modes.

For light of a given wavelength, λ_0 , in a material with a bulk refractive index of n , the propagation vector will have a total magnitude of

$$k = nk_0$$

where

$$k = \frac{2\pi}{\lambda_0}$$

This can be represented as circle in 2D k-space, requiring

$$k^2 = k_x^2 + k_y^2$$

Figure 28 shows the resulting diagram containing circles representing the allowed propagation vectors for both air and glass. The origin is considered to be at the physical interface, and as such, dashed lines are used to represent a propagation vector that is not allowed, due to the absence of the appropriate material. Thus, for propagation in air, is shown by the solid line to only be allowed in the lower half of k-space, and propagation in glass is shown by the solid line to only be allowed in the upper half of k-space, in effect representing the non-reciprocal space representation of the interface.

Thus, light scattered from the interface is only allowed to propagate with wavenumbers associated with the solid circles. However, the dashed lines are essential in order to represent the original incident light as a vector relative to the origin of k-space. Thus, in each of the following diagrams, the incident light is shown on the dashed circle, and the scattered light is shown on the solid circles.

For any dielectric interface, it can easily be proven that the transverse wavenumber must be conserved across the interface. Thus, the transverse wavenumber of the incident light is represented by the vertical dashed line. This line intercepts solid (allowed) portions of the two circles, indicating that light is allowed to travel in both directions, indicating the wavenumbers of both the transmitted and reflected modes from this interface. Note that this is nothing more than a geometric representation of Snell's Law, and the angles of the reflected and transmitted light agree with Snell's Formula, which in this material system can be written as

$$n_{glass} \sin \theta_i = n_{air} \sin \theta_t$$

The critical angle, defined as the incident angle from within the glass beyond which the light is totally internally reflected, can be found by inspection. It is the angle at which the transverse wavenumber of the incident light creates a dashed line that's tangent to the air circle. Beyond this angle, only one allowed mode exists, namely the reflected mode predicted by total internal reflection (TIR).

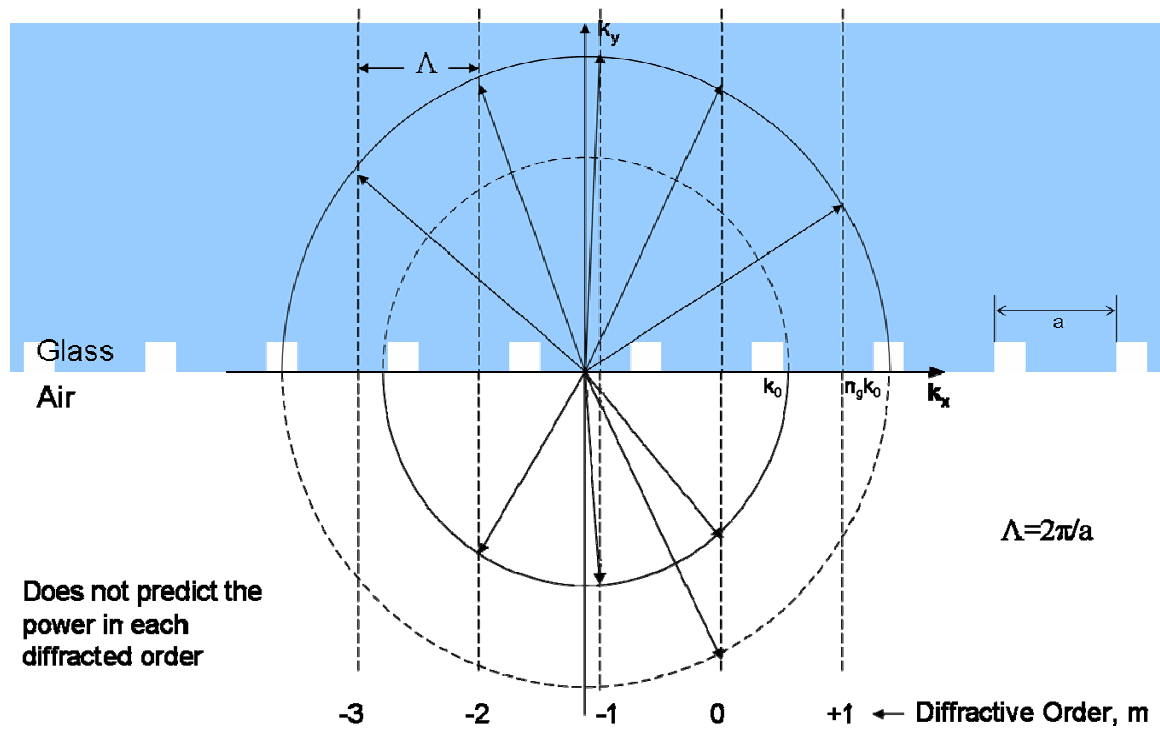


Figure 29. k-space representation of a transmission grating formed on a air/glass interface with the light incident from within the glass. Dashed lines represent the transverse wavenumbers of the supported diffractive orders.

This concept can be extended to the case of gratings. Gratings have the ability to modify the transverse wavenumber in discrete steps as determined by the period of the grating. If the grating is infinite in length, these additional allowed modes are narrow and evenly spaced, as shown in Figure 29. The incident light from within the glass is again shown on the dashed circle, and the transverse wavenumber is shown with a dashed line. The grating momentum is described by the grating pitch as

$$\Lambda = \frac{2\pi}{a}$$

and will serve to modify the transverse wavenumber in discrete steps with this periodicity. Each of these discrete steps is typically referred to as a diffractive order of the grating. Figure 29 shows the allowed diffractive orders, -3 to +1 of this grating. Note that there are a different number of reflected and transmitted orders, with the sign of the order being defined by the chosen coordinates of k-space. In this case, 8 diffracted orders are allowed, although this number will shrink as the physical dimension of the grating period is reduced. This results in a larger spacing between modes. Note that with a sufficiently small grating pitch, it's possible to have a single diffracted order, in addition to the reflected and transmitted modes.

Figure 30 extends this k-space concept to a waveguide. In this case, the waveguide core is silicon, and the cladding is silicon dioxide, resulting in circles with a radius of $n_s k_0 = 3.5k_0$ and $n_g k_0 = 1.5k_0$ respectively.

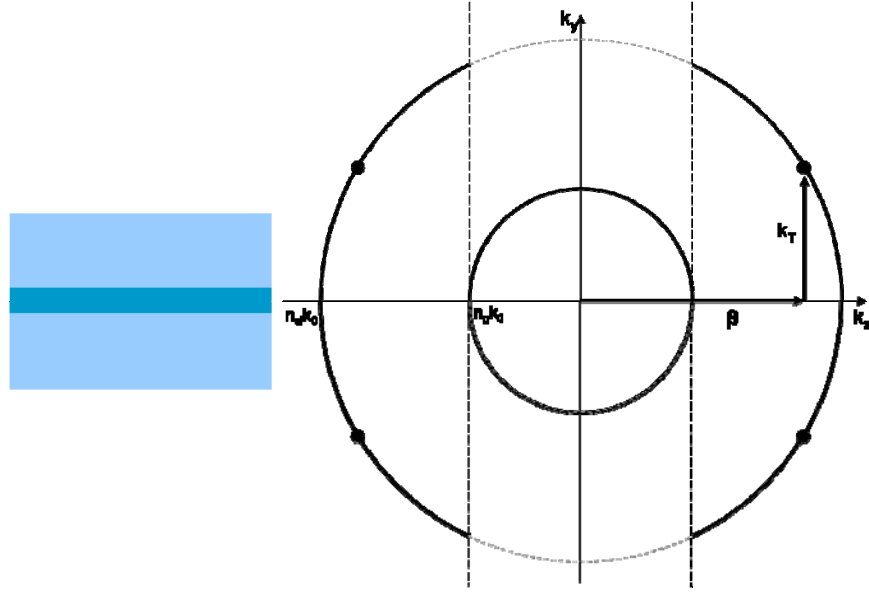


Figure 30. Cross-section of a slab waveguide and a 2D representation of the slab modes in k-space are represented by the points along the silicon circle. The dashed regions of the silicon circle represent regions where no TIR occurs, and waveguiding is not possible.

Note that since a waveguide requires TIR to operate, the only allowed region of k -space for waveguiding is where the transverse wavenumber of the core exceeds the tangent points of the cladding. Furthermore, in the waveguide itself, transverse resonant conditions dependent on the exact thickness of the waveguide film will reduce the allowed modes down to a select few, in this case with a periodic vertical wavenumber. In the example shown, it is presumed that the film thickness is chosen to allow only a single slab mode. In 2D k -space, this is represented by the 4 dots that intersect the allowed silicon k -space at the appropriate vertical wavenumber. (Note that when discussing waveguides, the transverse number of the slab waveguide is commonly known as what we're referring to here as the vertical wavenumber.)

Of course, the oxide cladding is present both on the top and bottom of the waveguide, and as such, light is allowed to travel in any direction in the cladding.

In 3D, each of the circles shown here becomes a sphere, and the slab waveguide mode becomes two parallel circles perpendicular to the page, and intersecting the sphere at the points shown.

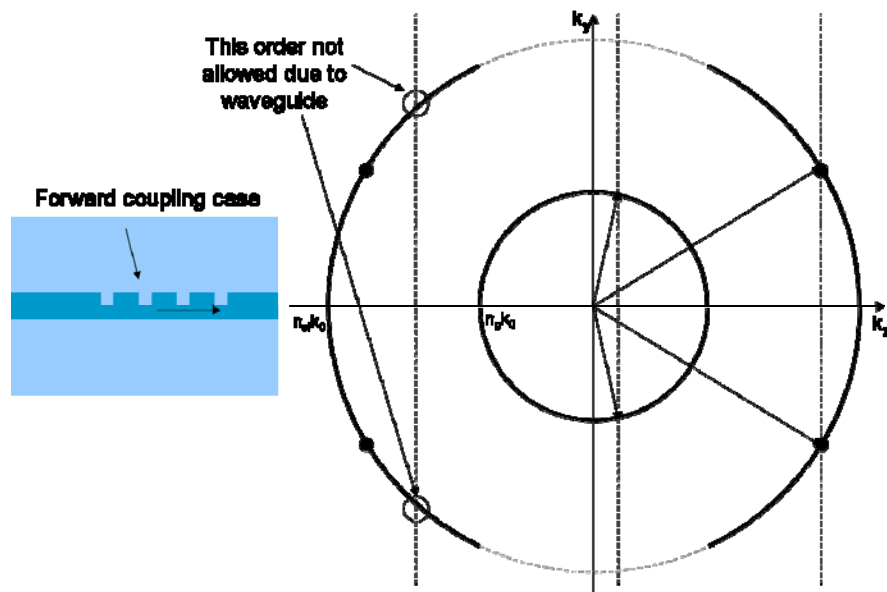


Figure 31. k -space diagram illustrating grating diffraction and waveguide modes.

Figure 31 shows a possible outcome when the waveguide is combined with a grating. In this case, known as forward coupling, the incident light is coming from above at a steep angle to the grating. Note that the light can momentarily enter the silicon and travel on through the bottom cladding. Also, a reflected mode is allowed in the upper cladding. If a grating was not present, there would be no other effect. However, the grating in this case is chosen to have a pitch

$$\Lambda = \beta - n_g k_0 \sin(\theta)$$

creating phase matching with a waveguide mode traveling in the positive direction. Note that while a diffracted order is present in the negative direction, it is not vertically resonant with the waveguide film, and as such, is not allowed to propagate. In this case, the light can be efficiently coupled to a single waveguide mode traveling in one direction. However, the transmitted and reflected modes still exist and will create waveguide coupling inefficiency.

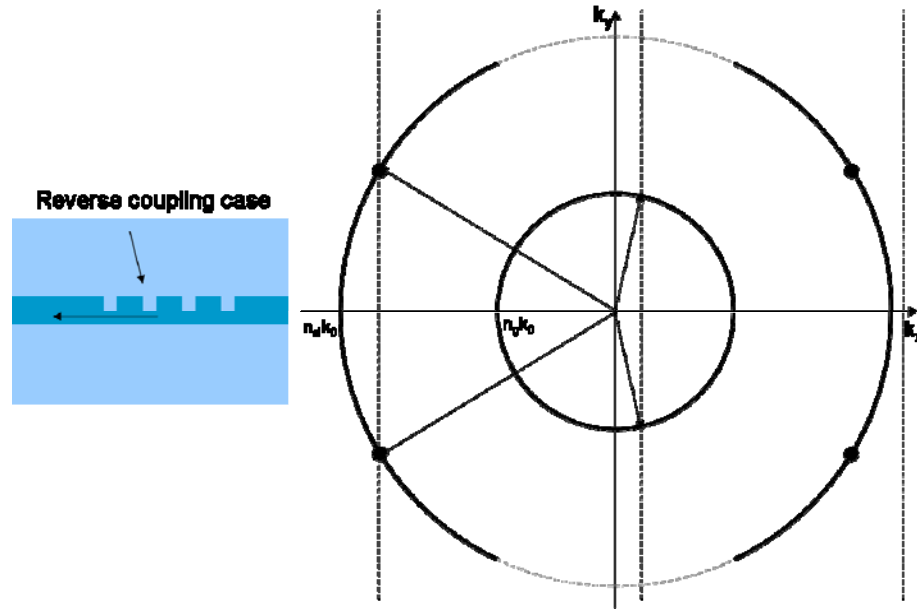


Figure 32. k-space diagram illustrating the reverse coupling condition where only one mode is allowed in silicon.

Figure 32 shows the grating coupler configuration known as backward, or reverse, coupling.

In this case, a slightly smaller grating period creates a condition where only a single allowed diffractive order intersects the silicon circle, and does so precisely at the negative traveling waveguide mode. Note that in this case, there is not even the possibility of coupling to a positively traveling mode as there is no allowed transverse wavenumber in that direction.

One interesting aspect to consider at this point is the potential bandwidth of these devices. The radius of the circle is defined by the wavelength of the incident light. Thus, these devices should only work for one precisely defined wavelength. If the grating were infinite in size, the k-space representation would reflect exactly this condition. However, due to the finite size of the gratings, the k-space representation of the allowed diffracted orders is broadened. However, due to the absence of any other allowed modes, this broadened k-space diffraction can still be highly efficient.

As the radius of the circles change with the frequency of the light, the grating momentum remains constant. In the forward coupling case, the reduced rate of transverse wavenumber walkoff will slightly extend the range over which the grating operates, and in the reverse coupling case, this will slightly reduce the range of operation. Also, note that the closer the rate at which the transverse wavenumber matches the change in beta, the greater the wavelength range over which the grating couples light into the slab.

For the forward coupled case, it's possible to match these numbers over a limited frequency range, or at least to design in such a manner that the difference is minimized. This technique allows design of grating couplers that are more broadband than a standard coupler. However, such a design suffers from the requirement to use a high incident angle, which is not always practical.

While this k-space approach allows selection for the periodicity of a grating coupler, it does not take into account several factors. First, mode matching to the desired output system is not considered. Second, the proportions of light contained in each of the output modes, transmitted, reflected, and waveguide coupled, are not considered. Finally, this is only a 2D

structure and does not consider the case of interfacing to a real 3D mode. These issues are addressed in a complete design methodology.

Grating Coupler Design Methodology

The baseline case indicated by the k-space argument is a uniform, periodic grating of a chosen periodicity. However, this model needs to be modified in a number of ways before design of an efficient grating coupler can be achieved. For purposes of this description, a single mode fiber will be considered as the desired optical system to interface with.

While in the previous section, the system was considered from the point of view of light incident on the grating from an external source. In the following discussion, the grating will be considered from the point of view of light in the slab waveguide, which will impinge on the grating and be scattered into the cladding regions. The reciprocal nature of the grating permits design from either perspective, and will create identical results.

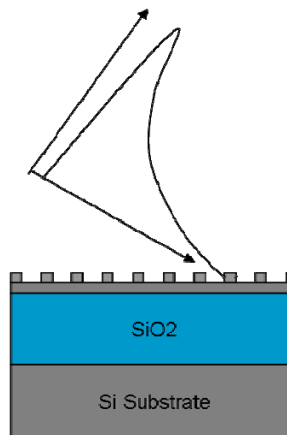


Figure 33. Exponential radiation profile from a uniform grating.

Gaussian Emission Profile

First, in order to mode match well with the Gaussian mode profile of a single mode fiber, it's necessary to change the scattering strengths of the individual scattering sites, henceforth referred to as "grates," such that the exponential function resulting from a uniform grating is transformed into the desired Gaussian distribution [19]. Figure 33 illustrates the nature of the

mismatch. In the strong scattering realm, where the amount of light remaining in the waveguide changes substantially upon interaction with each individual grate, the strength of the grates must be ramped, such that the product of the power incident on the grate, plus the scattering strength forms a Gaussian distribution, as illustrated in Figure 34.

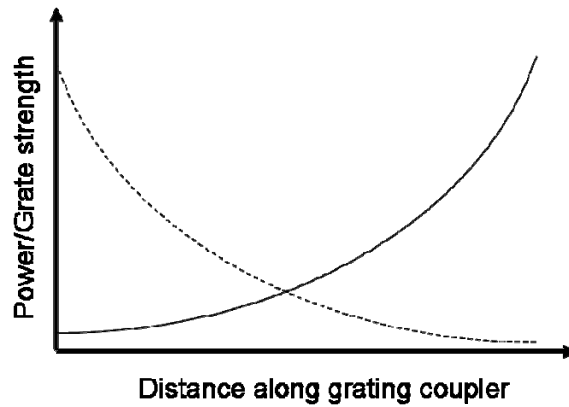


Figure 34. Illustration of relationship between power decay in the waveguide (dashed) and ideal grate scattering strength.

Grate Radiation Pattern

In order to prevent light from coupling to the radiation modes allowed in the bottom cladding, it's desired to design each individual grate in such a manner that the light is primarily scattered up. This can be modified by changing the thickness of the slab, and the depth of the etch into the slab. Additionally, it's sometimes desired to construct a grating from material deposited on top of the slab waveguide. In this case, the thickness of the original slab, and the index and thickness of the deposited material will influence the radiation profile from each grate. Figure 35 shows an example radiation profile from a 200nm thick film, with a 150nm thick polysilicon grating deposited on top. Note that light is scattered primarily up, although some light is also scattered down, and some light reflects back down the waveguide. In general, the less reflection, and the less light scattered down, the better the performance of an individual grate.

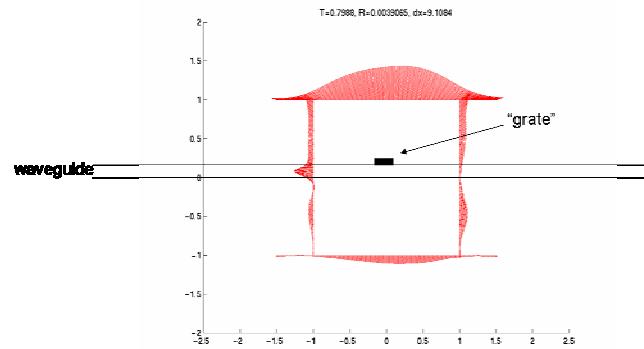


Figure 35. Radiation power scattered from a single “grate” deposited on a waveguide. Vectors indicate poynting flux through points along a box surrounding the grate. Note fraction of power scattered up.

Scattering Strength

In order to emit light within the small distance required by the cross-section of a single mode fiber, it's important that each individual grating be fairly strong, on the order of 10%. A typical transmission range is shown in Figure 36.

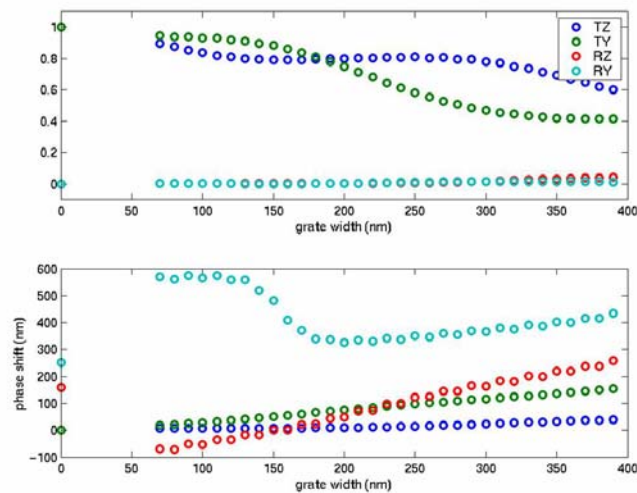


Figure 36. Scattering strength and phase shift as a function of grate width for both polarization modes of a slab waveguide. Note the nonlinear response of the functions. The vertical axis on the top figure shows both transmission and reflection coefficients for the two fundamental polarization modes of a slab waveguide. Scattered power is $1-T-R$.

Hyperbolic flare

The 3D nature of the fiber mode is compensated for by first expanding the waveguide in a hyperbolic flare, so that the transverse dimension of the grating matches the transverse dimension of the fiber at the location of the grating. While the transverse dimensions only perfectly match over a small range, this technique is superior to the linear expansion preferred in prior work. Expansion of a submicron waveguide into a large, $10\mu\text{m}$ waveguide is difficult, and requires a longer taper length than a simple hyperbolic flare. Thus, the grates follow the ellipses formed by the hyperbolic formula. Each focal point of the hyperbola corresponds to either the forward or backward coupling case. A picture of the resulting device is shown in Figure 37.

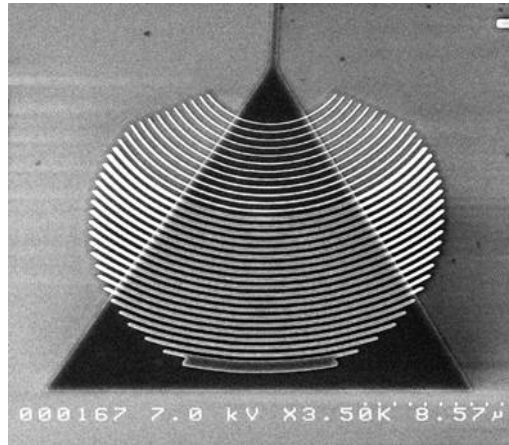


Figure 37. A SEM photograph of a grating coupler formed from polysilicon grates deposited on a hyperbolically flared silicon waveguide. The footprint of the grating represents a $10\mu\text{m}$ optical fiber mode. The output waveguide is $200\times 400\text{nm}$.

Variable Grate Phase Delay

As light is scattered from each grate, the amount of phase delay experienced changes. This can be calculated by comparison of the phase transmitted through a grate as compared to the case when the grate was missing from the waveguide. This is extracted by comparing the FDTD simulations of the two cases. An example phase delay through a range of grating lengths is shown in Figure 36. In order to maintain a constant phase shift, this results in a grating that is

semi-periodic, and that the ramp in periodicity is not necessarily a linear function of the grate dimensions.

Vertical Film Stack

Finally, it's possible to cancel out the mode directed at the substrate by reflecting it back towards the surface and using this light to cancel the reflected mode. As illustrated in Figure 38, the phase of this reflected light must be carefully considered, or destructive interference is created. However, when constructive interference is achieved, the efficiency of the device is greatly improved.

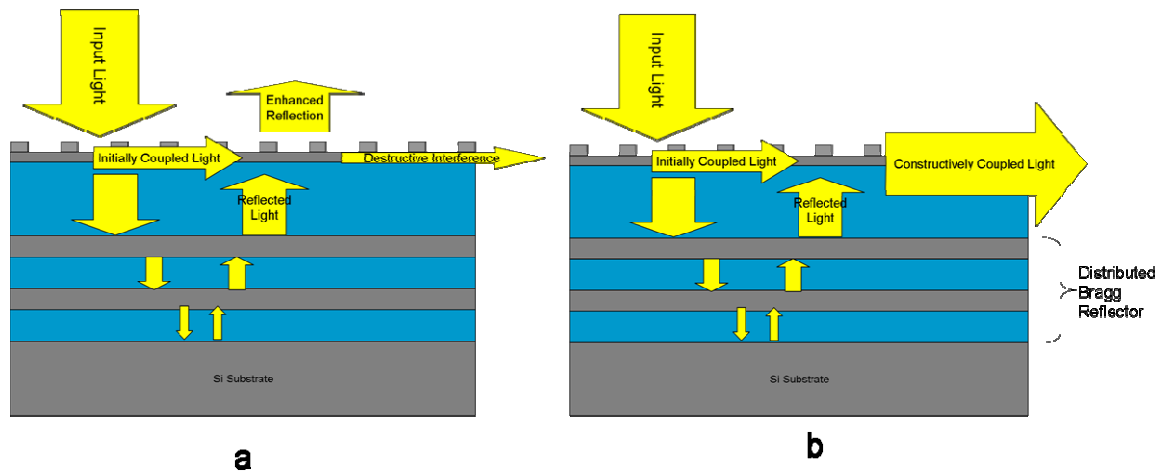


Figure 38. a) Destructive interference created by inappropriate choice of oxide thickness. b) Correct oxide thickness creates more efficient coupler. Any reflector will suffice, although DBR is shown.

Grating Library

For a given technology, represented by a silicon film thickness, minimum feature size, and a dimension of the scattering site, it's possible to construct a grate library, which is bounded on the smaller dimension by the lithographic capability of the process, and on the larger end by the required grating pitch. Within this range, the scattering strength, radiation profile, and phase delay can be captured. These simulations are typically performed using FDTD, as these parameters are difficult to extract analytically. However, once a grate library is constructed, the remaining grating design can be performed with a simple simulation tool, such as matlab.

Note that the grating library is also constructed as a function of wavelength, so that the spectral dependence of the scattering can be taken into account.

Each individual grating is placed in series, with the input to each successive grating being a function of the transmission of the previous gratings. The radiation profiles from each grating are then projected onto an upper and lower plane, where they are summed, taking into account their specific phases. Note that it's also possible to take into account the reflections from each grating, by including the transmission and reflection coefficients into a simple transmission matrix. Due to the physical symmetry of the simple gratings, the emission profile for the reflected component of light is simply the mirror image of the emission from the reflected light. After all contributions are summed, an emission profile for the light traveling up and down from the grating is constructed. The grating design can be optimized by taking the overlap integral of these modes with that of a fiber mode. The goal at this point in the design is to optimize the mode to more perfectly match a fiber mode for both the up and down traveling light.

Wafer Factor	Substrate Reflectivity	Modeled Peak Efficiency	Modeled Peak Efficiency (dB)
-1	-.16	.28	-5.5
0	0	.41	-3.9
1	.16	.54	-2.7
2	.74	.65	-1.9
3	.98	.67	-1.7
4	.99	.68	-1.7

Table 2. Simulated impact of substrate reflectivity on peak efficiency of an example grating coupler. Wafer factor refers to the number of reflective layers in the substrate. The negative number indicates a perfectly out of phase condition.

Subsequently, the light scattered down is recaptured by a thin film mirror designed to reflect the light upwards, combining it in phase with the originally upwards bound light. This part of the design can also be performed using a scattering matrix approach. After the design of the

grating is completed, a complex reflection and transmission coefficient of a fiber guided mode is extracted from light launched from both above and below the grating. Using these coefficients in a thin film scattering matrix allows modification of the remaining films to be done quickly and analytically, such that the design of thin films both above and below the grating can be considered. This approach has been verified with full FDTD simulations, although it's substantially faster in matrix form. In this manner, the fiber coupling efficiency of a grating coupler can be predicted for a variety of substrates. Table 1 illustrates a number of examples considered and the effect each substrate has on an example grating coupler. Note that the wafer factor of -1 is used to indicate the case where the reflected light is perfectly out of phase. A positive wafer factor indicates that the light is reflected in phase, which is the desired case.

CMOS PHOTONICS PLATFORM DEVELOPMENT

At this point in the project, most of the work transferred from Caltech to Luxtera. The devices shown from this point on were fabricated a Motorola's Semiconductor Products Sector, which later became know as Freescale Semiconductor. The fabrication capability developed over time from the simple process required to demonstrate grating couplers and waveguides to a complete integration of the technology with an existing CMOS process. Information contained in this thesis will cover the proof of principle work only, and will not consider the details of reliability, yield, and process stabilization required for product development.

Grating Coupler Realization

Using the combination of the above 2D design approaches, along with the hyperbolic flare gives the result shown in Figure 39. In this case, the available wafers had a buried oxide film thickness nearly perfectly anti-resonant with the grating, resulting in a wafer factor of -1. None-the-less, near perfect match between the predicted spectrum and the measurement result were achieved.

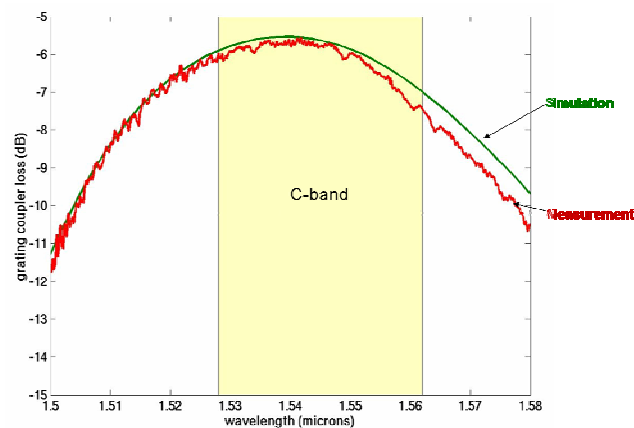


Figure 39. Simulation and experimental results from the first grating coupler design.

Measurement technique

Grating couplers are measured by constructing a short loop of waveguide connecting two identical grating couplers. A fiber array with the correct spacing to match the gratings is brought into close vicinity of the grating loop, and the transmission is optimized. After optimization, a wavelength scan is taken using a tunable laser. The measured loss experienced traversing two grating couplers is then halved to indicate the loss of a single grating coupler. Note that due to the short length of waveguide, $\sim 150\mu\text{m}$, waveguide loss is negligible.

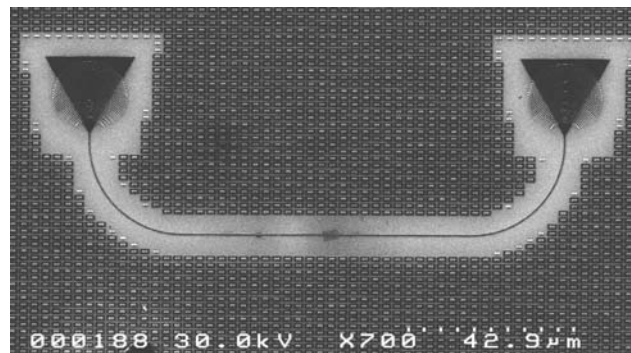


Figure 40. A test loop consisting of two identical grating couplers, connected by a short waveguide. Spacing is $127\mu\text{m}$.

Wafer-scale Test

One of the key advantages of using grating couplers is that it greatly enhances the ability to test optical devices. Instead of dicing, cleaving, and edge polishing devices before they can be tested, grating couplers allow wafers to be tested while fully intact. This allows the adoption of test equipment and methodologies standard in the electronics realm. Testing is performed using a standard wafer probe station, which has been outfitted with a fiber array that floats above the surface of the wafer. The positional accuracy of the stage is sufficient to allow single mode fiber alignment in just a few seconds using an active feedback loop. This allows rapid testing of thousands of points on a wafer to occur automatically. As a result, a testchip can contain thousands or tens of thousands of individual devices, each of which can be tested

without any modification or packaging activity. A photograph of the stage on the wafer probe station is shown in Figure 41.

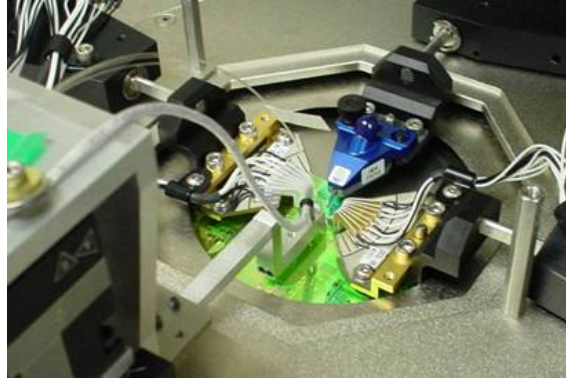


Figure 41. Photograph of wafer probe capability showing RF and low frequency electrical probes from the top and sides respectively. Optical fiber probe enters from the bottom of the picture. Fibers exit normally from the surface of the wafer and curve out of the picture on the left hand side. The wafer is the green surface below the probes.

This capability allows wafer mapping of key optical parameters, such as grating coupler efficiency shown in Figure 42. This allows correlation with processing parameters and other sources of variability to be studied, so that problems can be diagnosed and better understood. For example, the ring pattern shown in this wafer plot indicates that the peak efficiency is experiencing an impact from a film deposition know to have this signature.

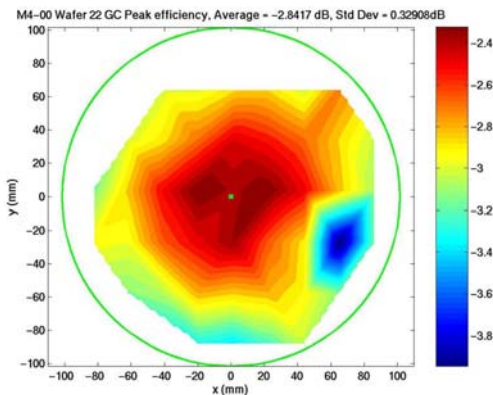


Figure 42. Wafer plot of peak grating coupler efficiency as an example of the benefits of wafer-scale testing.

Ring resonators

Ring resonators are very interesting components for use as filters and modulators. Their simplicity, combined with their small size makes them a compelling option for implementation in a system architecture based entirely on rings. Furthermore, use of rings for measurement of waveguide loss and effective index makes them useful diagnostic tools to be employed in a small area within a wafer.

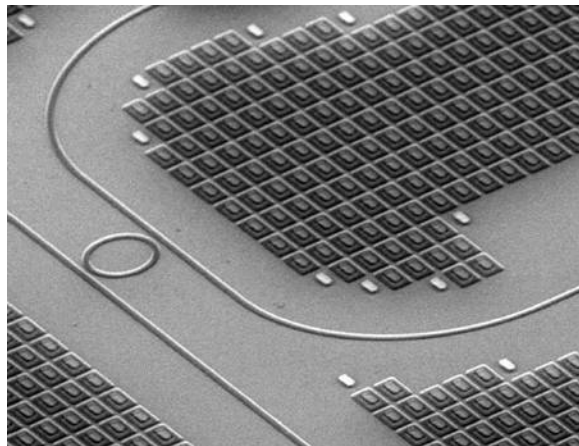


Figure 43. Ring resonator configured as an add/drop filter. The ring diameter is $5\mu\text{m}$.

Ring Resonators as Filters

When used as a filter, a ring resonator is typically deployed between two waveguides, as shown in Figure 43. When the frequency of the light is on resonance with the cavity frequencies of the ring, and if the coupling coefficients are well matched between the ring and the waveguides, the light is transferred from the input waveguide to the output waveguide. This effect is well known, and the ring resonator architecture was a cornerstone technology for several transient optical communications companies during the late 1990s, such as Little Optics and Nanovation. Despite impressive technical progress, none of these companies managed to develop a lasting value proposition. Never-the-less, they did advance ring resonator architecture such as the development of multi-pole ring filters, effectively solving the free-spectral-range and crosstalk issues associated with ring filters when used for demanding telecommunications applications.

Free Spectral Range

The FSR of a cavity is the separation between adjacent resonances, which is determined by the physical geometry of the cavity, and is given by the formula

$$FSR = \frac{c}{n_e 2\pi r}$$

This is plotted in Figure 44 as a function of optical pathlength. Three significant optical pathlengths are called out: 100GHz is the typical channel spacing used in communications systems today, 4THz is the width of the optical C-band, which contains 40 channels, and 195THz is the frequency of 1550nm light. Note that in order to convert to ring radius, the optical pathlength needs to be divided by $2\pi n_e$, which is approximately 20. Thus, to have a single ring capable of isolating an individual wavelength over the C-band, the radius of that ring must be less than $\sim 3.75\mu\text{m}$!

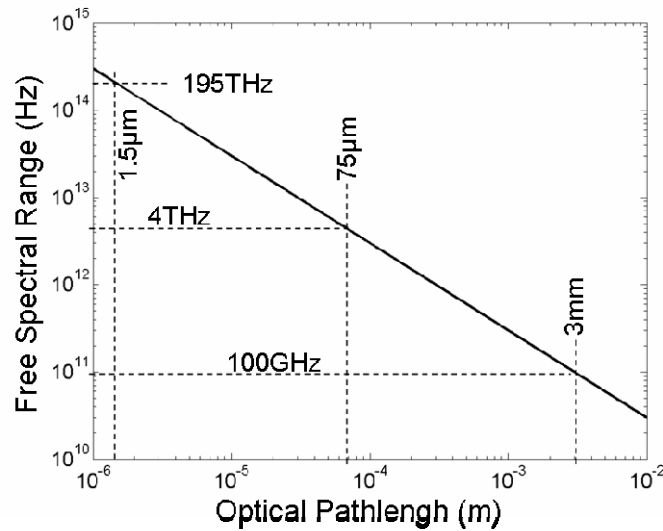


Figure 44. Effective optical pathlength vs. cavity FSR, and the required cavity length for several interesting frequency spans.

Single Pole Filter Design

A particularly advantageous configuration for ring resonators is when a single ring can be employed as a filter. This eliminates the problems inherent with manufacturing a matched pair

of rings, and avoids the crosstalk associated with the control algorithms for multiple rings.

Figure 45 illustrates the case when a ring with a Q of 10,000 is used as a single pole filter for channels with 100GHz spacing. The crosstalk between adjacent channels is -20dB in this configuration, which is acceptable for a data link, assuming the link is capable of handling the associated power penalty. To minimize distortion, it's desired to have the Q of a ring used as a filter as low as possible, while trading off the impacts on the link penalty due to adjacent channel crosstalk. This allows some room for misalignment in addition to minimizing the distortion link penalty.

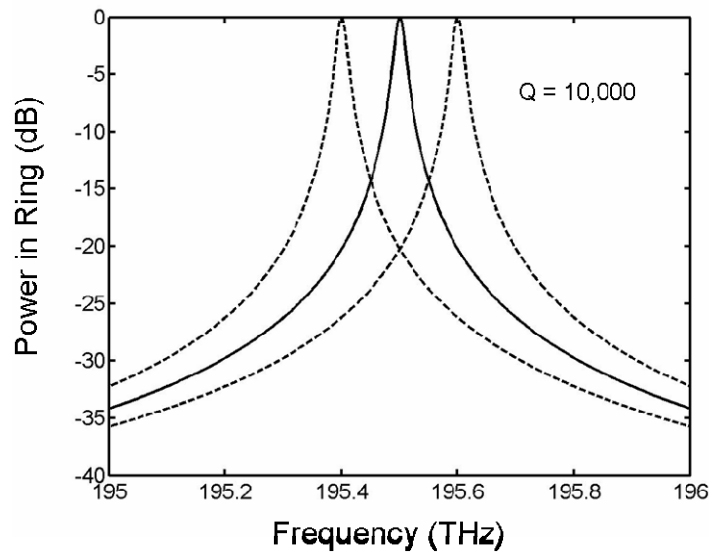


Figure 45. Filter shape of ring with $Q=10,000$. Adjacent channels plotted with dashed lines, demonstrating -20dB crosstalk with each adjacent channel.

For most applications, a total crosstalk of about -15dB is an acceptable value to ensure minimal impact on the link performance.

The Q of 10,000 was chosen to pass both sidebands of a 10Gb signal within a 3dB rolloff, however, this will have a non-negligible impact on the fidelity of the link. Figure 46 shows the link power penalty impact for a ring resonator, including the additional impact of misalignment with the signal. In the case of 10Gb transmission through a ring of $Q=10,000$, a distortion

penalty of 1.3dB is calculated, so this is likely an upper bound on the desired Q . In practice a tradeoff will be made to find the optimal link power penalty as a function of Q . As the Q gets higher, the power penalty increases for the filtered signal due to distortion and clipping of the content towards the edges. As the Q is reduced, the crosstalk at a given channel spacing increases. However, the example given here is proof that a workable solution exists around 100GHz channel spacing for a Q of $\sim 10,000$.

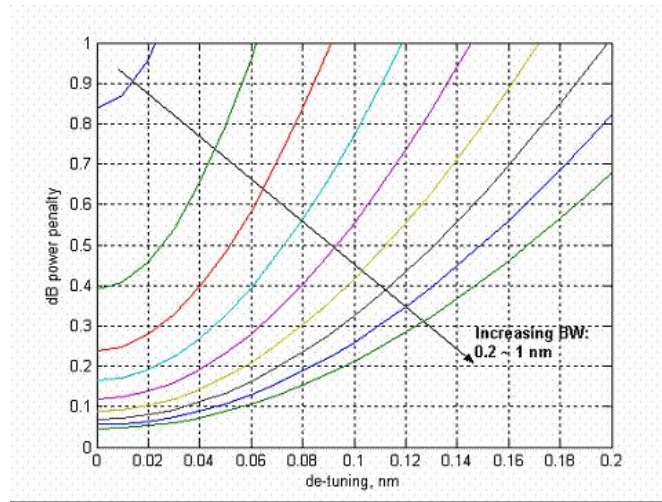


Figure 46. Calculation of power penalty as a function of bandwidth and misalignment for a ring resonator.

For 10 channels with a spacing of 100GHz, the FSR of the single ring needs to be about 1THz, which means that a radius of ~ 15 microns is required, clearly defining the need for high-index contrast waveguides for a ring-based architecture.

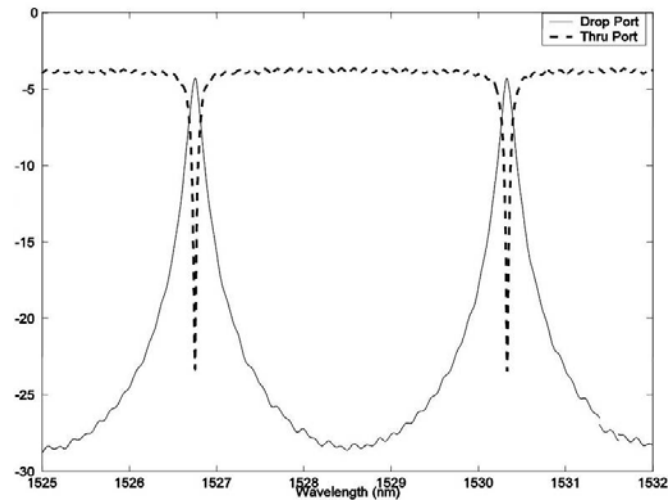


Figure 47. Data taken from the drop and transmission ports of a ring filter. Vertical axis in dB.

This sets the motivation for a 15 micron radius ring with low insertion loss, and a Q of about 10,000. Figure 47 shows the test results for a ring resonator configured for multiplexing. This particular device was designed for 10Gb data, and with a FSR capable of handling 4 channels, spaced 100GHz. The Q for the device was 10,900, higher than the target of 10,000. This allows a passband of 18GHz, which will slightly clip the double sideband 10Gb data. In order to increase the passband, the device should be more strongly coupled to the input and output waveguides. The FSR of the ring was 450GHz, which is more than adequate for a 4-channel multiplexer. Note that the loss on the dropped wavelength was quite small, <0.5 dB. The 4dB background loss results from fiber coupling on and off the chip. These numbers represent fiber-to-fiber insertion loss of a packaged device.

Rings have also been evaluated for the possibility of single pole operation over the entire C-band. The inset in Figure 48 shows a ring resonator formed in 200nm thick slab of silicon, etched completely through, and with a $2\mu\text{m}$ bend radius. The test results from this ring are shown in Figure 48. The resulting FSR was 45nm, more than enough to span the entire C-band, which is only 32nm wide. Note that this ring was only measured in a single waveguide configuration. The Q of this ring was 22,000, however, as the second waveguide is added to

the configuration, the Q of the system would necessarily drop, reducing the Q to a level defined by the design of the couplers.

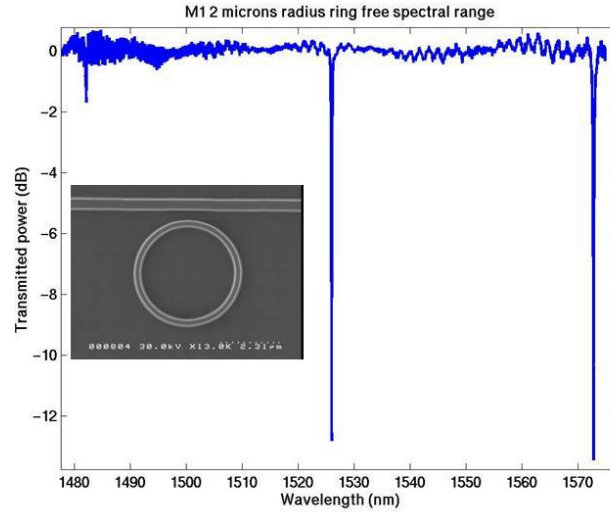


Figure 48. Transmission measurement of a $2\mu\text{m}$ radius ring, creating a 45nm (56THz) FSR. Inset shows measured ring and waveguide.

Rings as Diagnostic Structures

Ring resonators can also form a compact structure for measurement of optical properties of waveguides. One parameter that's difficult to directly measure is the effective index of a waveguide. However, if a ring is corrugated at a periodicity of half the propagation wavevector, coupling between the counter propagating modes will occur. In this case, there is an additional loss mechanism for this mode only. Thus, if one designs a ring to be slightly overcoupled to an adjacent waveguide, it is expected to see low extinction ratio resonance dips for the majority of the modes, but for the mode corresponding to the periodicity of the ring, it is expected to see an increased extinction.

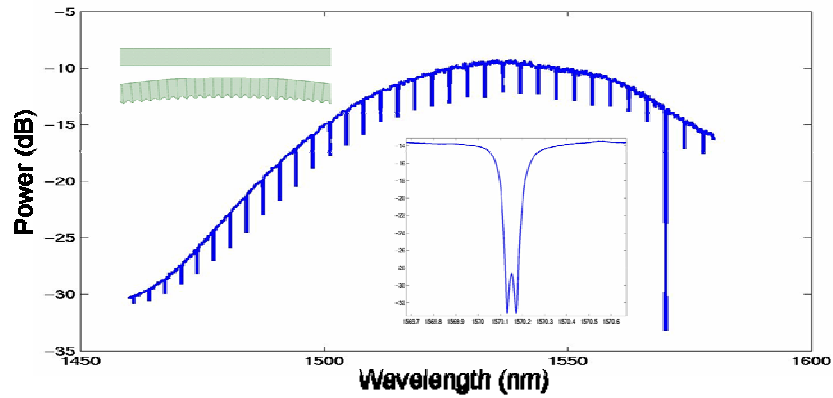


Figure 49. Spectrum of a corrugated ring showing critical coupling at the resonance order associated with the corrugation period. Upper inset shows coupling region of ring structure. Lower inset shows close up view of deep resonance.

Figure 49 shows measurement results from one such ring. Note that the resonance of the coupled mode is split, as predicted by theory. This allows determination of the precise mode number observed in the ring. With this information, the remainder of the resonances can be used to extract the effective index, and consequently the group index as well. The excellent correlation between the ring measurements and measurements taken from the reflection of straight corrugated waveguide are shown in Figure 50.

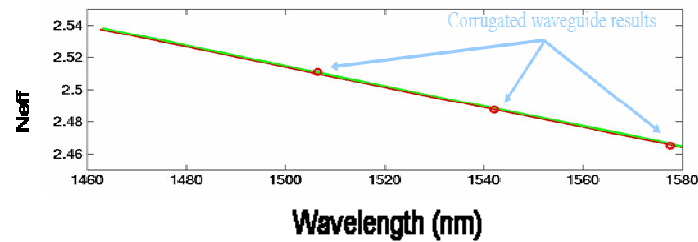


Figure 50. Corrugated waveguide measurements (red dots) plotted with continuous curves extracted from ring measurements.

Rings as Modulators

The design of a ring to be used for a modulator is substantially different than one used for mux/demux. First, consider that the ring is being used to provide amplitude modulation of the light. Thus, it's intentionally perturbing the transmission of the light, whereas a filter's

objective is to pass the light with minimal distortion. Second, in order to minimize the tuning range required for modulation, the ring should be as high Q as possible, while still maintaining an optical rise/fall time compatible with the bit rate.

In order to be compatible with a time constant of 20ps, a ring requires a Q less than 24,500. A ring with a Q of 20,000 has a time constant of 16ps, which makes a good target for 10Gb operation. Figure 51 illustrates the time constant of a ring as a function of Q for operation at 195THz, or $\sim 1.55 \mu\text{m}$.

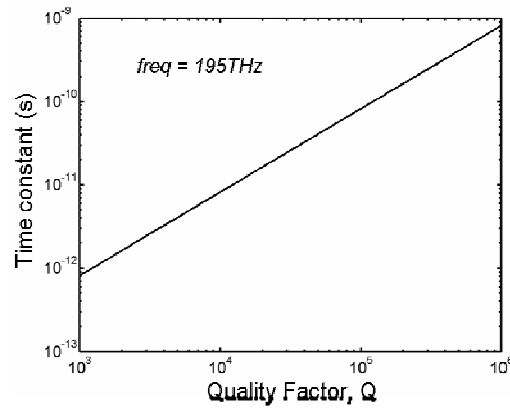


Figure 51. Time constant of a cavity as a function of Q for 1.55 μm light.

There is a fundamental tradeoff between Q and the amount of index modulation achievable. Fundamentally, the fraction of the resonant frequency that can be moved is exactly proportional to the fraction that the wavelength of the light in the waveguide can be changed. Since the wavelength of light in the waveguide is determined by the effective index, n_e , it's correct to say

$$\frac{\partial n_e}{n_e} = \frac{\partial f}{f}$$

However, note that $\partial f/f$ is $1/Q$. Thus in order to move the ring a distance equivalent to the 3dB bandwidth, the required effective index change can be easily approximated by

$$Q = \frac{n_e}{\partial n_e}$$

For a ring with a Q of $\sim 20,000$, this means that an index modulation of 50 ppm is required. For an effective index of 2.8, the absolute effective index change required is then 1.4×10^{-4} .

A complicating factor is that a ring is often not modulatable around the entire circumference. The coupling region is typically left unmodulated, and there is an additional requirement for a slower bias modulator in order to tune the ring to the correct operation wavelength. This means that the index modulation required is inversely proportional to the coverage of the ring by the high speed modulator. Thus, a ring with 50% coverage needs 100ppm of index modulation in order to function ideally.

CMOS Modulator

Basic Free-Carrier Modulation Properties of Silicon

The basic equations governing free carrier modulation in silicon were first published by Soref in 1986 [1]. Derived from the Drude model and the Kramer-Kronig relations, these equations describe an intrinsic relationship between index modulation and absorption.

$$\Delta n = -\frac{e^2 \lambda^2}{8\pi^2 c^2 \epsilon_0 n} \left[\frac{\Delta N_e}{m_{ce}^*} + \frac{\Delta N_h}{m_{ch}^*} \right]$$

$$\Delta \alpha = -\frac{e^3 \lambda^2}{4\pi^2 c^3 \epsilon_0 n} \left[\frac{\Delta N_e}{m_{ce}^{*2} \mu_e} + \frac{\Delta N_h}{m_{ch}^{*2} \mu_h} \right]$$

where n is the index of refraction, e is the electron charge, λ is the free space wavelength of the affected light, c is the speed of light, ϵ_0 is the permittivity of free space, ΔN is the change in carrier concentration, μ is the mobility, and m^* is the effective mass. The subscripts e and h denote coefficients for electrons and holes, respectively. Experimental evidence published in

Soref's paper implied the need for three correction factors, which perturb these equations from theory as follows

$$\Delta n = -\frac{e^2 \lambda^2}{8\pi^2 c^2 \epsilon_0 n} \left[\frac{\Delta N_e}{m_{ce}^*} + \frac{\Delta N_h^{0.8}}{m_{ch}^*} \right]$$

$$\Delta \alpha = -\frac{e^3 \lambda^2}{4\pi^2 c^3 \epsilon_0 n} \left[4 \frac{\Delta N_e}{m_{ce}^{*2} \mu_e} + 2 \frac{\Delta N_h}{m_{ch}^{*2} \mu_h} \right]$$

The impact of holes on effective index has been found to be less than linear, and the absorption measured from both electrons and holes was found to be 4 and 2 times greater than predicted by theory.

For these curves, experimental data was fit with

$$m_{ce}^* = 0.26m_0$$

$$m_{ch}^* = 0.39m_0$$

Using known values for these parameters, and $\lambda = 1.55\mu\text{m}$ results in the following simplified relations [60]:

$$\Delta n = -(8.8 \times 10^{-22} \Delta N_e + 8.5 \times 10^{-18} \Delta N_h^{0.8})$$

$$\Delta \alpha = 8.5 \times 10^{-18} \Delta N_e + 6.0 \times 10^{-18} \Delta N_h \text{ (cm}^{-1}\text{)}$$

Of course, α can be converted to dB/cm by multiplying by 4.34.

Note that only the absorption term contains a mobility term. This has potential significance in the event that SiGe, or strained silicon can be employed with this technology, effectively reducing the inadvertent loss associated with the phase modulation. However, this has not been verified by any known experiments.

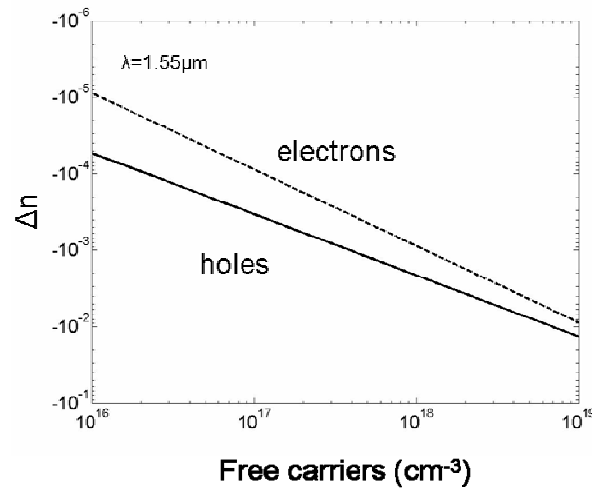


Figure 52. Index modulation as a function of free carrier density from Soref's corrected formulas.

The refractive index and absorption changes as a function of carrier density are shown in Figure 52 and Figure 53 respectively. Note that holes have a substantial benefit, having both a larger index modulation, and a smaller absorption over the carrier concentrations of interest for reverse biased operation.

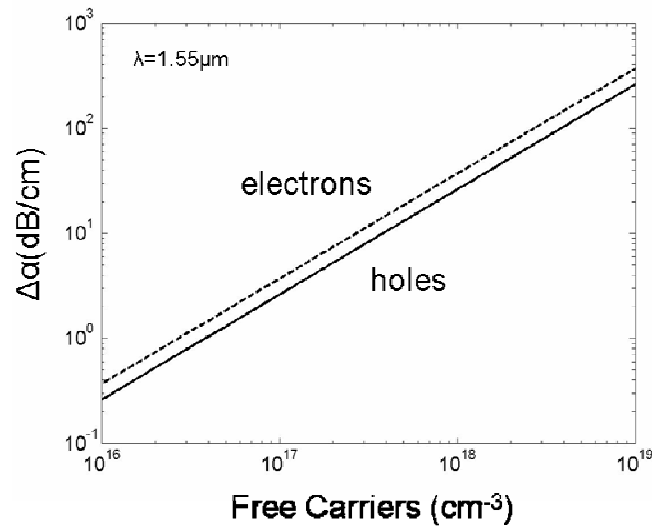


Figure 53. Absorption modulation as a function of free carrier density from Soref's corrected formulas.

A key metric to consider is the ratio of index change to absorption. This effect is substantially larger for holes than for electrons. As shown in Figure 54, there is an advantage when using lower concentrations of holes. For electrons, the ratio is constant and substantially worse, only 1.04×10^{-4} . This absorption to index change ratio should be kept in mind when designing MZI modulators, where an imbalance in power between the two arms will be created by this absorption, limiting the achievable extinction ratio.

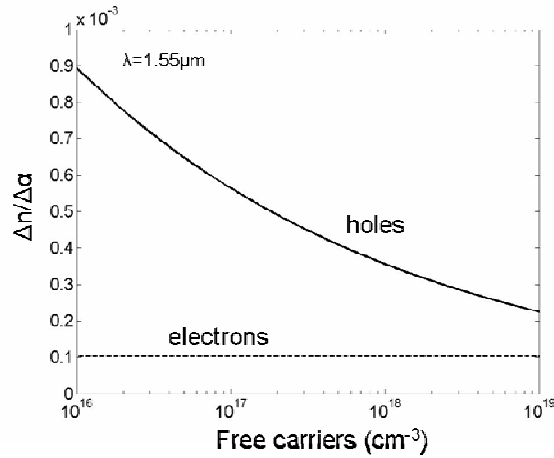


Figure 54. Ratio of index modulation to loss by free carriers.

It's also important to keep in mind that the refractive index of silicon has a substantial thermal coefficient, which at $\lambda = 1.55 \mu\text{m}$ is given to be $\partial n / \partial T = 1.86 \times 10^{-4} \text{ K}^{-1}$. This should be considered when using forward biased junctions, or other devices where there is a significant amount of power dissipation.

Diode Basics

Since the basic operation of the modulator involves application of voltage to modify the size of the depletion region, it's worth giving some considerations to this effect.

The width of a depletion region for an abrupt p-n junction is given as [61]

$$W = \sqrt{\frac{2K_s \epsilon_0}{q} \frac{N_A + N_D}{N_A N_D} \phi_T}$$

where K_s is the dielectric constant of silicon at electrical frequencies, 8.86×10^{14} F/cm, q is the electric charge, N_A and N_D are acceptor and donor concentrations, and ϕ_T is the total potential applied to the diode, given by

$$\phi_T = \phi_B + V_R$$

where V_R is the applied reverse bias voltage, and ϕ_B is the built-in potential, given by

$$\phi_B = \frac{kT}{q} \left(\ln \frac{N_A}{n_i} + \ln \frac{N_D}{n_i} \right)$$

where k is Boltzmann's constant, 8.62×10^{-5} eV/K, and n_i is the intrinsic carrier concentration, which is $1.45 \times 10^{10} \text{ cm}^{-3}$ in silicon.

Thus, the size of the depletion region is fixed by the material and doping concentrations, and varies with temperature and applied voltage. Combining these equations provides

$$W = \sqrt{\frac{2K_s \epsilon_0}{q} \frac{N_A + N_D}{N_A N_D} \left(V_R + \frac{kT}{q} \left(\ln \frac{N_A}{n_i} + \ln \frac{N_D}{n_i} \right) \right)}$$

Examining this equation clearly shows both a bias dependent, and a temperature dependent term.

The nature of the depletion region is sensitive to the doping profile in the immediate vicinity of the junction. While the abrupt junction can be used to derive a physical intuition of the depletion region, the actual performance is dependent on the exact physical profile, and thus cannot be precisely described analytically. In practice, the profile of the junction can be extracted from CV measurements of the reverse-biased junction.

The Waveguide

The final concept that must be considered when creating a model for a silicon modulator is the waveguide itself. In general, since the modulation will be a strong function of the fraction of the waveguide experiencing depletion region modulation, a small waveguide is desired.

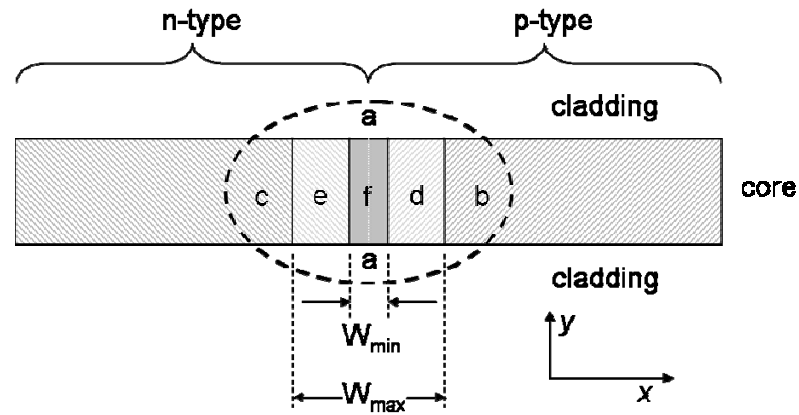


Figure 55. Cross-sectional diagram of a generic modulator waveguide. Guiding mechanism not shown in order to focus on modulator itself.

A generic waveguide is shown in Figure 55. The light is assumed to travel into the page, down the depletion region of the diode. Light is guided in one of six positions, a) the waveguide cladding b) the static p-implanted waveguide c) the static n-implanted waveguide d) the p-dynamic depletion region, e) the n-dynamic depletion region f) the static depletion region. The dynamic regions are defined as the minimum and maximum extents of the depletion boundary under bias voltages.

Obviously it's ideal to have the mode entirely confined to the dynamic regions of the depletion region, regions e and d. In order to maximize this overlap, the static depletion region, f, should be minimized, the voltage should be maximized, and the light should be confined to as small of an area as possible, paying particular attention to the transverse wavenumber in the x-direction, which will determine the amount of confinement in the dynamic regions.

It is possible to assume that the shape of the optical mode does not change significantly during modulation, as the amount of index change is quite small, $\sim 10^{-4}$, which will have a negligible

impact on the transverse wavenumbers, and hence the confinement factors of the different regions.

The depletion width of a diode vs. doping concentration is given in Figure 56 for several voltages. The dashed line represents the state with no applied voltage. Note that around the design range of interest, $\sim 10^{17}$, as we will see later, the depletion region is 175nm across with no reverse bias. Thus, a substantial amount of optical power is present in the dead zone, f. With a 2V swing, approximately 125nm of additional waveguide is exposed, meaning that for a symmetrically doped diode, regions d and e each move by ~ 60 nm. Thus, it's very important that the waveguide mode be tightly confined. Also, there is a substantial benefit to slightly forward biasing the diode. While care should be taken to avoid injection of minority carriers due to their long lifetime, the phase modulation per Volt is greatest when the diode is closest to forward bias. However, this must also be considered in context of the operational requirements and overall design of the modulator. Specifically, since the capacitance of the diode increases in this range, the modulator must be designed specifically to operate in this regime.

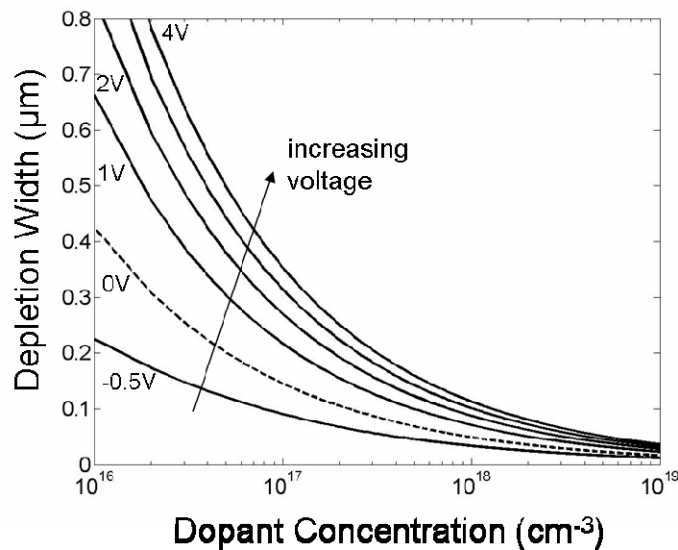


Figure 56. The movement of the total depletion width as a function of concentration and voltage. Shown for -0.5, 1, 2, 3, and 4V.

Now we can describe both the phase and amplitude modulation of this phase modulator in terms of confinement factors, Γ , in the different regions of the device. First, consider the propagation wavenumber, β , in light of Γ

$$\beta = \frac{2\pi}{\lambda_0} \left(\Gamma_a n_{clad} + \Gamma_b n_b + \Gamma_c n_c + \Gamma_d (n_b - \Delta n_h) + \Gamma_e (n_c - \Delta n_e) + \Gamma_f n_f \right)$$

Given a set voltage limit for a '1' and a '0,' the extents of the dynamic regions, d and e, of the modulator are well defined and fixed. Since the goal of this work is integration into a CMOS environment, which has firm limits on voltage swing, this type of simplification is appropriate. This reduces most of the terms in this equation to constants, leaving only the Δn terms, which will be considered as a function of doping concentration.

Similarly, the loss of the waveguide can be written as

$$\alpha = \alpha_0 + \left(\Gamma_a \alpha_a + \Gamma_b \alpha_b + \Gamma_c \alpha_c + \Gamma_d (\alpha_b - \Delta \alpha_h) + \Gamma_e (\alpha_c - \Delta \alpha_e) + \Gamma_f \alpha_f \right)$$

where α_0 is the scattering loss of the passive waveguide, which is presumed to be identical to a doped waveguide. Measurements of waveguide loss are done for each doping concentration, providing quantitative input for the attenuation coefficients of this equation, again leaving only the $\Delta \alpha$ terms associated with the free carrier movement.

In reality, a modulator waveguide has a mechanism to confine the light tightly in the region of the diode junction. This is accomplished by using a rib waveguide as shown in Figure 57.

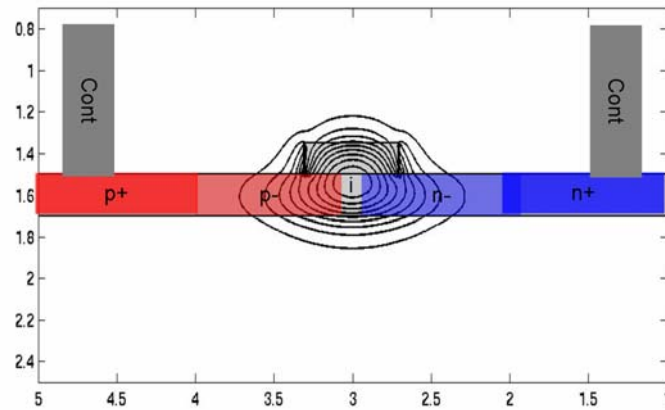


Figure 57. Cross-sectional view of a silicon modulator. The optical mode is shown along with the overlap with the implants. This does not reflect doping in the ridge portion, although the ridge is typically doped as well.

This structure can be formed many ways, although it's currently implemented by etching a thick film down in order to form the guide. Selective growth of the rib, deposition of polysilicon, and etching the top film of a double stack wafer have all been considered. The double stack film approach has been implemented, although this design was bandwidth limited, and the modulation efficiency is reduced by not allowing carriers to impact the optical power present in the upper portion of the rib. Using the etched rib approach, additional modulation efficiency and higher bandwidth is achieved.

Modulator Measurement Results

The modulator is measured using a signal generator, a Bit Error Rate Tester (BERT), a commercially available modulator driver, and a high speed oscilloscope, such as an Agilent DCA. Differential signals are applied to the different arms of the modulator, and the optical power is measured with an optical plug in module for the DCA. The modulator diodes can be DC biased through use of a bias tee, and 50Ω loads are required at the termination of the modulator.

By repeating this measurement for a range of voltages and recording the wavelength shift of the interference points, it's possible to accurately extract the phase shift as a function of applied voltage. Simultaneously, it's possible to confirm that there's little, if any, wavelength dependence for this effect. Figure 60 shows the extracted phase shift as a function of voltage. The implant density used was $1\text{e}17\text{cm}^{-3}$, although the curve fits the $2\text{e}17\text{ cm}^{-3}$ line more closely. Additionally, the simple theory [61] predicts a \sqrt{V} dependence, however, the observed measurement fits a $V^{2/3}$ slope. Both effects are easily explained by diffusion of the dopants in the junction region due to high temperature steps during the silicon processing.

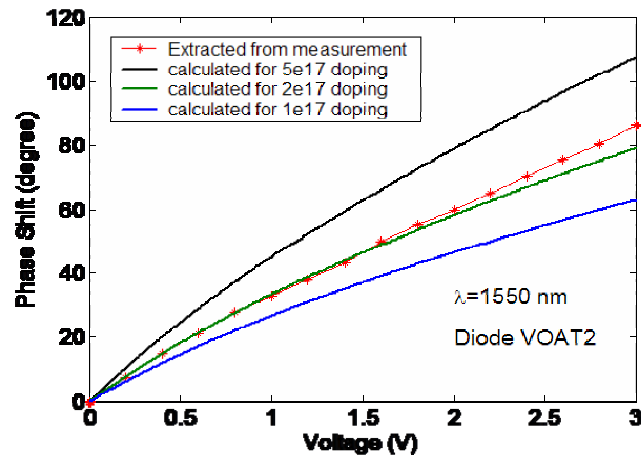


Figure 60. Modulator phase shift as a function of DC voltage for a 5mm device.

High speed measurements have also been performed, both a small signal frequency response measurement and an eye-diagram formed from digital data. The results are shown in Figure 61. The 3dB frequency response is 10GHz, and the modulator rolls off quite evenly beyond this frequency. This modulator has also been tested with a random bit pattern and the resulting eye diagram is shown in the inset.

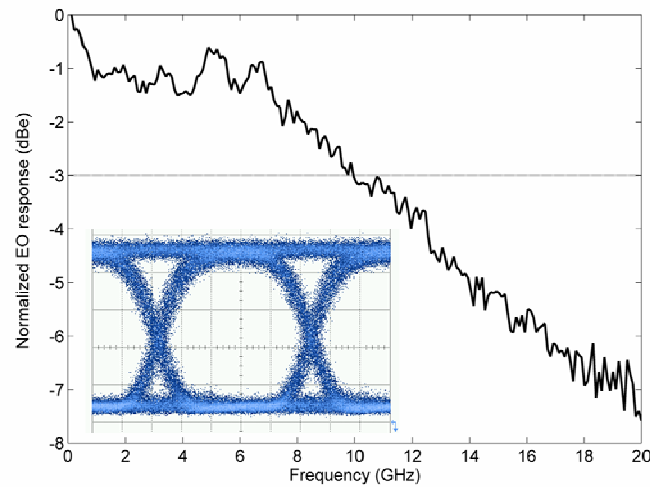


Figure 61. Frequency response measurement and 10Gb eye diagram for a reverse biased modulator.

Wafer Selection

Double Stack Wafer

Integration of both optical and electrical functionality on a single wafer couples the design of the transistors and the design of the optical devices. There are basically two straightforward options available a) keep the film thickness of the original transistor process and design the optics accordingly b) modify the film thickness and recharacterize the resulting transistors. While option a is best from a transistor point of view, it turns out to be nearly impossible with the film thicknesses used in $0.13\mu\text{m}$ SOI transistors, which turns out to be $\sim 100\text{nm}$. Optics, ideally would be fabricated in films several times this thickness. The solution to this problem is a third option, called the double stack wafer, as shown in Figure 62.

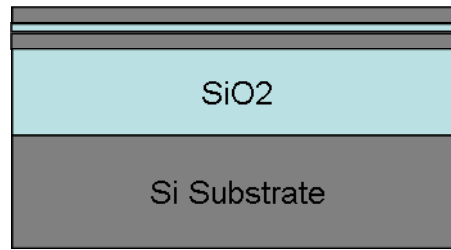


Figure 62. Cross-section of a double stack wafer. A thin oxide breaks the top silicon electrically, but maintains single mode operation optically.

Conceptually, this is a thick SOI film optimized for optical performance, with a thin, electrically-isolating oxide layer placed in the middle. This film serves to cut the film electrically, although it's thin enough that the optical performance is not significantly impacted. Thus, the best performance for optical structures is attained while preserving the desired film thickness for the electronics.

This wafer has other advantages as well. First, the middle oxide layer serves as an etch stop, allowing the dimensions of the resulting waveguides and grating couplers to be controlled more precisely. Second, the unpatterned bottom silicon layer allows electrical contact to the lower portion of the waveguide, allowing electrical contacts for forward and reverse biased p-n modulators, as well as resistive heaters. This allows the contact plugs to be placed well away from the optical modes, reducing the scattering and absorption created by the salicided contact regions, while maintaining a low resistance path required for high speed modulation.

A number of separate fabrication runs were attempted with this wafer geometry. Grating couplers, high speed modulators, and transistors were all fabricated, however, this wafer was difficult to manufacture, and eventually became impossible to procure. This led to development of a process to optimize a single silicon film SOI wafer for simultaneous construction of transistors, modulators, and grating couplers.

Optimization Process

In order to determine the optimal wafer to integrate the complete set of optical and electrical functionality into, a detailed process was undertaken. It was important to consider both the

impact of the film thickness of the performance of transistors in addition to the optical properties of modulators, waveguides and grating couplers. Furthermore, it was important to optimize the design so that a single etch could be used for definition of the waveguides and the scattering sites of the grating coupler. This process is necessary to ensure no misalignment between the two features, and to simplify design and processing.

Three basic wafer structures were considered. One used a top film thickness of 100nm, identical to the transistor process. However, this thin film confined the light poorly, and the mode extends towards the substrate. Thus, in order to avoid substrate leakage, it required an extremely thick buried oxide layer of 1.8 μ m, making wafer fabrication quite difficult. The silicon film would be etched completely through in order to simultaneously define transistor bodies and all optical features. The major drawback of this option was the need for innovative structures in order to make electrical contact to the core of the waveguide. Concepts like a segmented waveguide, which consists of a periodic conductive bridge designed to minimally impact the optical mode were explored, but appear to be challenging to implement.

The second main class of wafer was the double stack wafer, but reconstructed at a more capable wafer vendor. This wafer had the advantages described above, but required a difficult and unproven manufacturing process.

The final option was to choose a film with an increased silicon thickness, and develop transistors in this film alongside the optics. The advantage of this technique was the ease of contact to the modulators, but etch depth could not be accurately controlled, creating design issues for waveguide effective index and grating coupler efficiency.

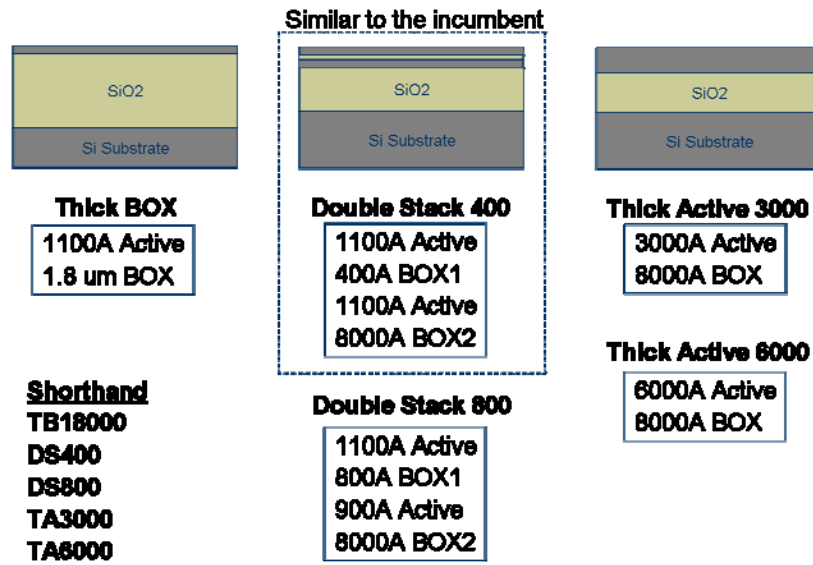


Figure 63. The 5 wafer options considered for production implementation.

The 5 main wafer options are summarized in Figure 63. Each of these options was considered based on 5 main criteria, wafer manufacturability, waveguide performance, grating coupler performance, and modulator performance. It was known that integration of transistors was possible in any of these films, so this was left to be modeled after the number of options was reduced.

Waveguide performance was considered by modeling and considering waveguide effective index, the index contrast between core and cladding, and the potential for optical loss. When considering effective index, it's important to also consider the sensitivity of this index to etch depth or CD controls, so that phase errors in the waveguides across the surface of the wafer can be controlled. A lower effective index, meaning light has a longer wavelength inside the waveguide, simplifies grating coupler design, while higher effective index makes grating coupler design more difficult. The index contrast is important to consider since higher index contrast allows tighter bend radius at a given optical loss. While these parameters can be directly calculated, waveguide loss cannot. This was estimated based on measured results from prior fabrication runs and published literature. The waveguides were then ranked in each category, and a total ranking was constructed from an unweighted sum of all categories.

Wafer	Effective Index	Rank	Eff. Index Sensitivity	Rank	Index Contrast	Rank	Loss (dB/cm)	Rank	Total Ranking
TB18000	1.99	1	0.82	5	0.34	1	unknown	3	2
DS400	2.46	2	0.34	1	0.17	3	5-10	4	1
DS800	2.50	3	0.50	4	.20	2	Similar to DS400	5	5
TA3000^a	2.85	4	0.44	2	0.12	5	Good potential	2	3
TA6000^b	3.15	5		3	0.15	4	Best potential	1	4

Table 3. Composite ranking of waveguide performance by wafer type.

The outcome of this activity is summarized in Table 3. The default wafer, the DS400, had the best composite score due to manufacturing variation tolerance, although it was known to have a poor waveguide loss. The worst wafer was the DS800, which sacrificed manufacturing sensitivity while maintaining a poor optical loss.

The second main consideration was the grating coupler. This depended on the nature of the scattering sites that could be constructed. The etch depth for the scattering strength was tied to the etch depth for the waveguide definition in the previous section. For the grating coupler, only the efficiency of a simple 2D grating was considered. For each case, the design methodology describe above was taken, but was limited to 2D simulations. Again, the DS400 wafer was the best scoring wafer, with 66% efficiency, as can be seen in Table 4. The DS800 and TA3000 wafers both had the same efficiency, so the etch depth repeatability was used to break the tie. The worst score was taken from a thin SOI wafer with polysilicon grates fabricated on top. Note that by the time the thickness of a single slab of silicon reaches 600nm, the grating coupler efficiency has dropped off dramatically due to the inability to correctly form the required deep scattering sites.

Wafer	Grate Type	Efficiency	Ranking
TB18000	Etched slots	55% ^a	4
TB18000	1200Å Poly ribs	40% ^a	7
TB18000	2000Å Poly ribs	52% ^a	5
DS400	Etched slots	66%	1 ^b
DS800	Etched slots	65%	2
TA3000	1050Å STI	66%	3
TA6000	2250Å STI	49%	6

^a The BOX effect has been estimated

^b The DS options don't require a well calibrated STI, which broke the tie
All simulations performed with .18um minimum active feature size

Table 4. Ranking of grating coupler efficiency for the wafer types.

Finally, the modulator was considered based on simulations of the 50% modal area (in square microns), the confinement factor of the light in silicon, the dimensions of the optimum waveguide, and the transverse wavenumber of the waveguide. Each of these is an important input into modulator design, as they reflect the size, shape, and ability to modulate the light. Actual modulator design was determined to be too time consuming for each of the options, so optimization of a small, well laterally confined mode was performed instead. In this case, the TA3000 wafer was the clear winner, as the film thickness and waveguide CD could be optimized to confine the light more tightly when all inputs were considered simultaneously.

Wafer	50% Mode Area	Rank	Si Conf. Factor	Rank	Guide CD (nm)	Rank	Trans. Wavenumber	Rank	Total Ranking
TB18000 ^c 1200Å Poly	0.049	2	0.39	4	310	5	3.50	5	6
TB18000 2000Å Poly	0.055	2	0.36	6	250	6	4.03	1	5
DS400	0.088	4	0.40	3	600	2	3.78	2	2
DS800	0.0900	5	0.36	5	700	1	3.60	4	4
TA3000 ^a	0.080	3	0.44	2	430	4	3.61	3	1
TA6000 ^b	0.100	6	0.83	1	525	3	3.50	6	3

Table 5. Wafer types ranked by key modulator performance parameters.

When all the inputs from each major category were collated and the wafers were ranked, the TA3000 wafer had the winning score. Note that it is not the best option for any of the individual performance criteria, but that when compared in a composite manner, it outperformed all other options. This is a good compromise wafer, which when considered alongside the potential for manufacturability made this wafer the clear choice. At this point, all development activities transferred to the TA3000 wafer.

Wafer	Wafer Manufacturability	Waveguides	Grating Couplers	Modulators	Total Ranking
TB18000	3	2	4	NO	7
TB18000 1200A Poly	3	2	7	6	6
TB18000 2000A Poly	3	2	5	5	5
DS400	5	1	1	2	2
DS800	4	5	2	4	4
TA3000	1	3	3	1	1
TA6000	2	4	6	3	3

Table 6. Final ranking of the different wafer types.

Many of the results given in the prior sections rely on measurements taken from the TA3000 wafer. Using this wafer has resulted in the high speed modulators previously mentioned. Figure 64 shows a comparison of the double stack wafer modulator versus the modulator based on the thicker film. Note that while the 3dB rolloff of the TA3000 result has been improved from 3GHz to 10GHz, the rolloff of the DS400 wafer was less steep at higher frequencies. The eye diagram on the TA3000 wafer, however, is much cleaner with faster rise/fall times, and an improved eye opening ratio. Another key difference between the two wafers was the implementation of a high resistivity substrate, which is responsible for much of the improved frequency response.

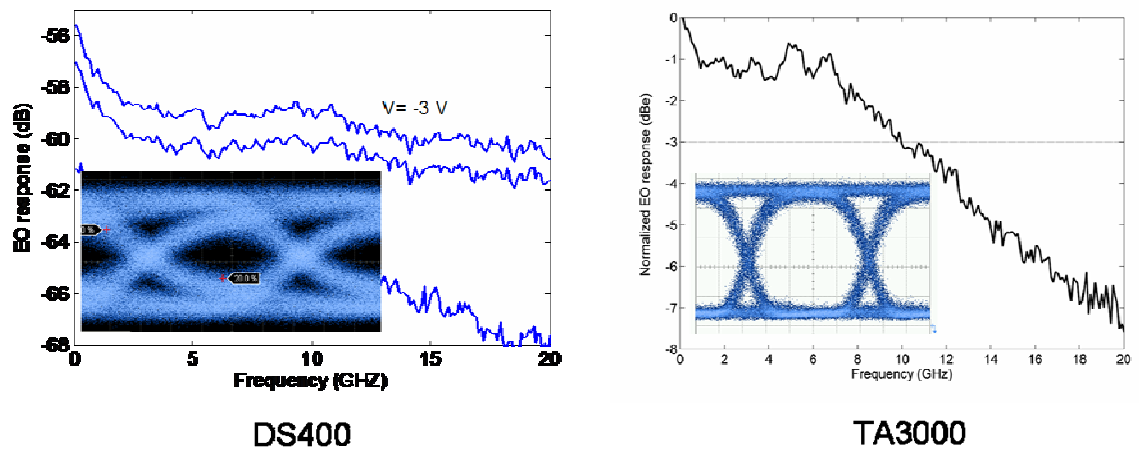


Figure 64. Comparison of frequency response and 10G modulator eye diagrams on different wafers.

Additionally, grating couplers have evolved into very efficient devices. Figure 65 contains a series of measurements made as the grating coupler design evolved. The bottom line was the best result from the first lot, and over time continued improvement occurred. The second to bottom line was essentially the same design as the first, but used a correct buried oxide layer, and was constructed in the DS400 wafer. The third line from the bottom was an evolved design in DS400, and the best measurement result shows the improvements achieved by moving to the TA3000 wafer and continued fine tweaking of the grate library. The best simulated design shows a performance of -0.3dB, and relies on additional reflectors constructed in the wafer, as shown in Figure 38, in addition to near perfect transfer of the mask design onto the wafer.

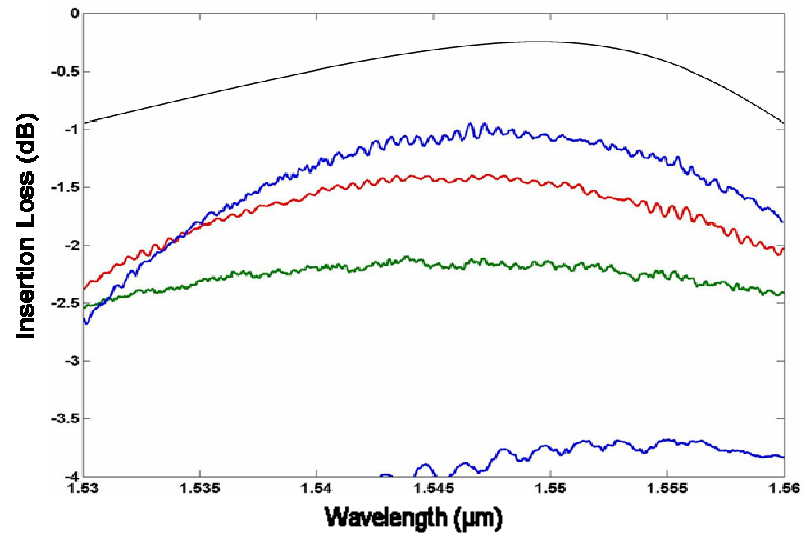


Figure 65. Grating coupler insertion loss over the C-band. Top line indicates best simulation result. Other lines are measurements showing evolution over time.

In addition, waveguide loss has been reduced to in the TA3000 wafer. The DS400 wafer was providing loss in the range of 5-8dB/cm. Figure 66 shows the results for TA3000. The loss is averaging 1.8dB/cm, although it can be reduced by using multimode waveguides down to ~ 0.5 dB/cm.

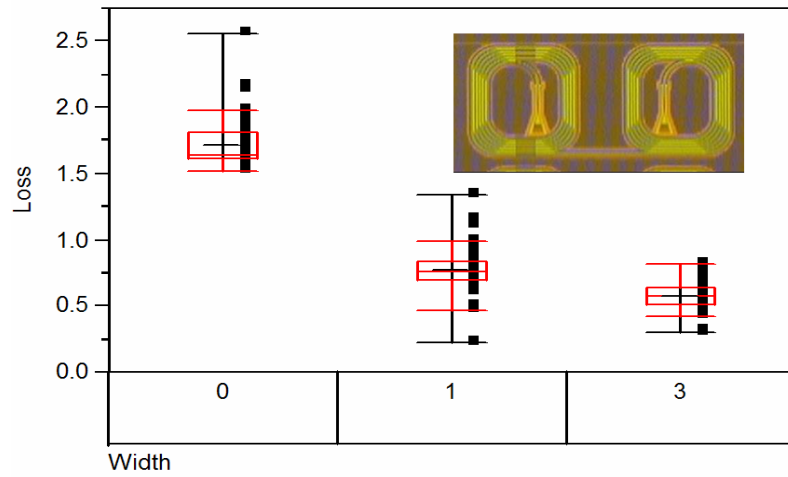


Figure 66. Waveguide loss for the nominal waveguide width of $0.5\mu\text{m}$, compared to waveguides $1\mu\text{m}$ and $3\mu\text{m}$ wide. Note the decreasing loss with additional width. The 500nm width is guaranteed to provide single mode operation. The average loss is 1.8dB for this configuration. Inset: A waveguide “scroll” used in varying lengths to extract loss.

The TA3000 wafer has proven to generate exceptional transistor performance and optical performance simultaneously. Waveguide loss, modulation efficiency, and grating coupler efficiency have all been enhanced with this design.

CONTINUED WORK AND FUTURE PROSPECTS

Dimensional Scaling

Integration of photonic capability into CMOS is exciting because it allows the technology to scale in a superlinear fashion while continuing to drive down costs. Of course, this scaling can only continue to occur if the size of the individual components continues to decrease. Figure 67 shows the scaling required to integrate increased bit rates on a transceiver die 1cm square. A 100Gb part consists of 10G transceivers, each less than 3x3mm in order to fit this on a single die. A 1Tb part requires each 10G transceiver to be 1mm square. Of course, this is making the assumption that 10G is the standard cell for all future development. Note that at 10Tb, a transceiver needs to be 316x316 μm . This is not an outrageous dimension in light of the resonant cavity architectures, such as ring resonators or photonic crystal cavities, which simultaneously provide optical multiplexing and modulation.

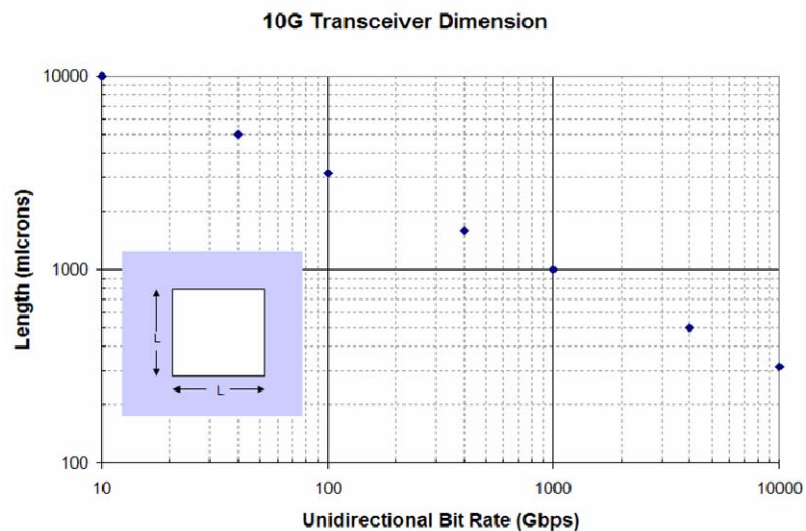


Figure 67. Scaling for dimension of each 10G transceiver assuming numerous 10G transceivers are used to attain a significantly higher unidirectional bit rate. Based on a 1sq. cm die.

The Bandwidth Limitations

One interesting question to consider is what impact silicon-based photonic technology will have on the fundamental limitations of communications bandwidth. Figure 68 represents the major bounding constraints on optical bandwidth from a materials point of view. The bandwidth of SMF-28 is limited both by the material absorption, and by the single-mode cutoff frequency. The other limitations are materials systems, and it can be seen that there's a substantial overlap where the available III-V light source technology, silicon transparency window, and the Germanium detector capability all overlap.

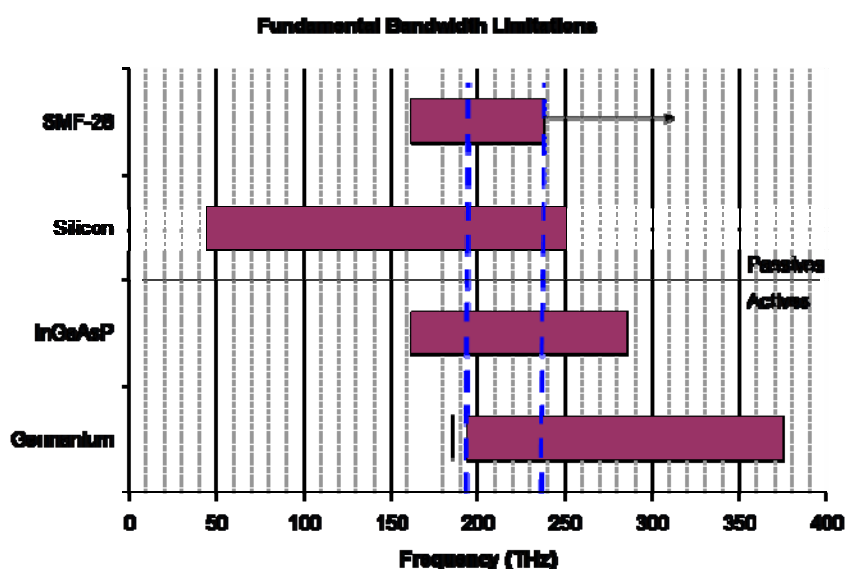


Figure 68. Fundamental limitations of silicon photonics technology from a materials and media perspective. The bandwidth between the blue lines represents the addressable bandwidth, ~45THz. This can be extended up to another 10THz by straining the Ge to redshift the absorption edge.

Today's WDM systems attain 0.10bits/Hz spectral efficiency by spacing 10Gb payloads every 100GHz. Ultradense systems attain 0.20bits/Hz efficiency by utilizing a 50GHz spacing for the same payload. Due to the availability of plentiful bandwidth, optical systems have not been driven to acquire the same spectral efficiency that RF communications has, but it's quite reasonable to make the assumption that 0.25 bits/Hz can be achieved. This indicates that the technology ultimately has the potential to place 10Tb of data in a single fiber.

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